

MS-7522M1

ATX Version: 2.0

CPU: Nehalem-EP 1S, BloomField Processors In LGA1366 Package.

System Chipset:

Intel Tylersburg I/O Hub 36S (North Bridge)
Intel ICH10R (South Bridge)

On Board Device:

CLOCK Gen -- ICS 9LPRS133
LPC Super I/O -- Fintek F71882FG
Dual LAN --Realtek 8111C
HD Audio Codec -- RTL888/888 VC
PCIE to 1PATA/2SATA Bridge -- JMB-363
1S to 2S HW RAID-- Bridge JMB322 (1S interface from JMB-363)

Main Memory:

3-Channel A / B / C DDR-III * 6

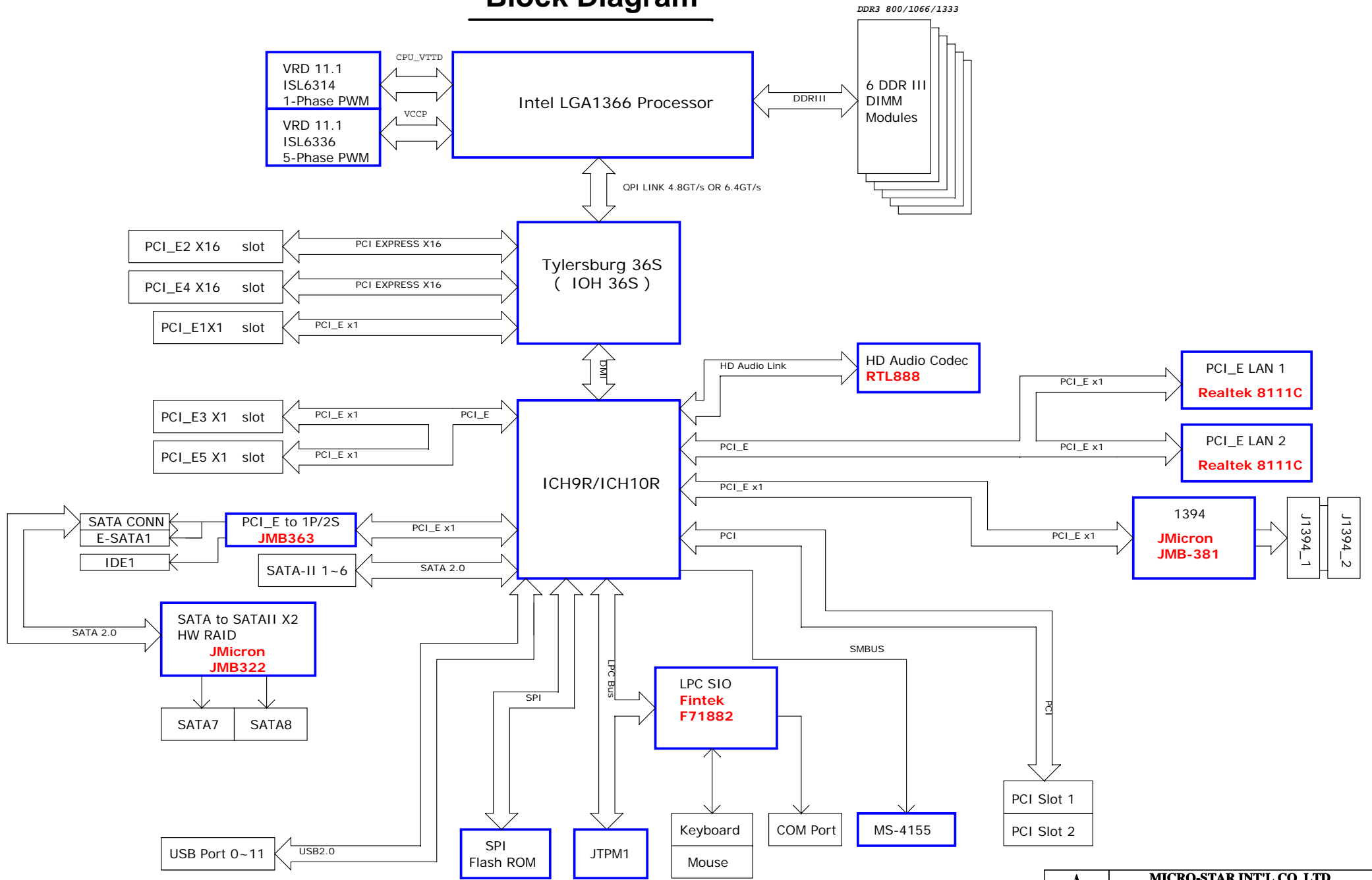
Expansion Slots:

PCI EXPRESS X16 SLOT *2
PCI EXPRESS X1 SLOT*3
PCI SLOT * 2

PWM: VR11.1 Intersil ISL6336 (5 Phases)

CONTENT	SHEET
Cover Sheet, Block Diagram	1-2
Intel LGA1366 CPU	3-8
DDR3 Chanel-A / Chanel-B / Chanel-C	9-11
Intel IOH 36S	12-19
ICH10R	20-22
Clock Gen ICS9LPRS133	23
PCI SLOT1 , 2	24
PCI-E X16 SLOT1 , 2	25
PCI-E X1 SLOT 1, 2, 3	26
SIO-Fintek F71882FG	27
LAN1 / LAN2 - RTL8111C	28-29
Audio Codec ALC888	30
1394 Controller - VT-6308	31
JMB-363 - E-SATA X1/ IDE X1	32
JMB-322 - RAID SATA X2	33
USB Connector	34
VRD11.1 - ISL6336 5-Phase	35
Phase Dropping & DOT	36
CPU_VTT - ISL6314 1-Phase	37
ACPI Controller UPI	38
NB Core Power & DDR Power	39
ATX Connector / Front Panel	40
ICH SATA X6 / FAN Control	41
GPIO Controller / EMI	42
XDP PORT/ Manual Parts	43-44
GPIO Setting / PCI Routing / Power Map	45-46
Reset & PWROK Map / 6-layer PCB Stack-up	47-48
Revision History	49

Block Diagram



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MS-7522

Size Custom	Document Description BLOCK DIAGRAM	Rev 2.0
Date: Tuesday, October 21, 2008		
Sheet 2 of 49		

9 DATA_A[0..63] <<>

10 DATA_B[0..63] <<>

11 DATA_C[0..63] <<>

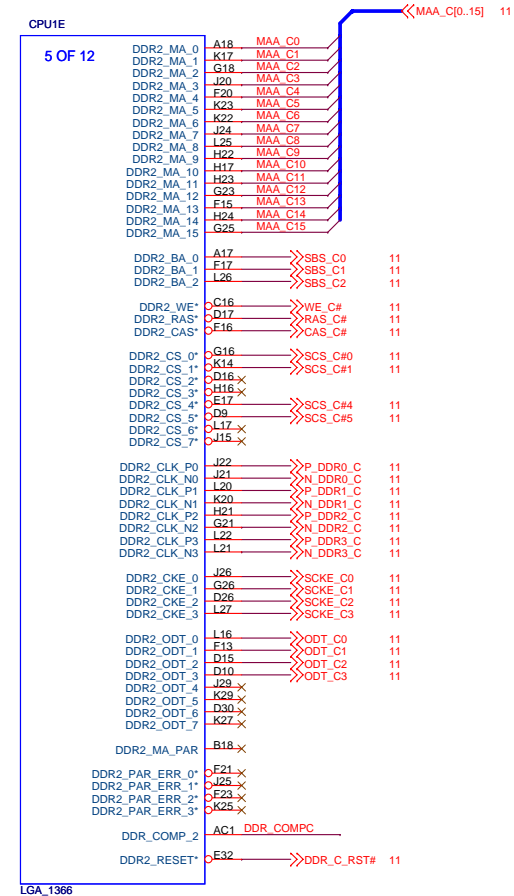
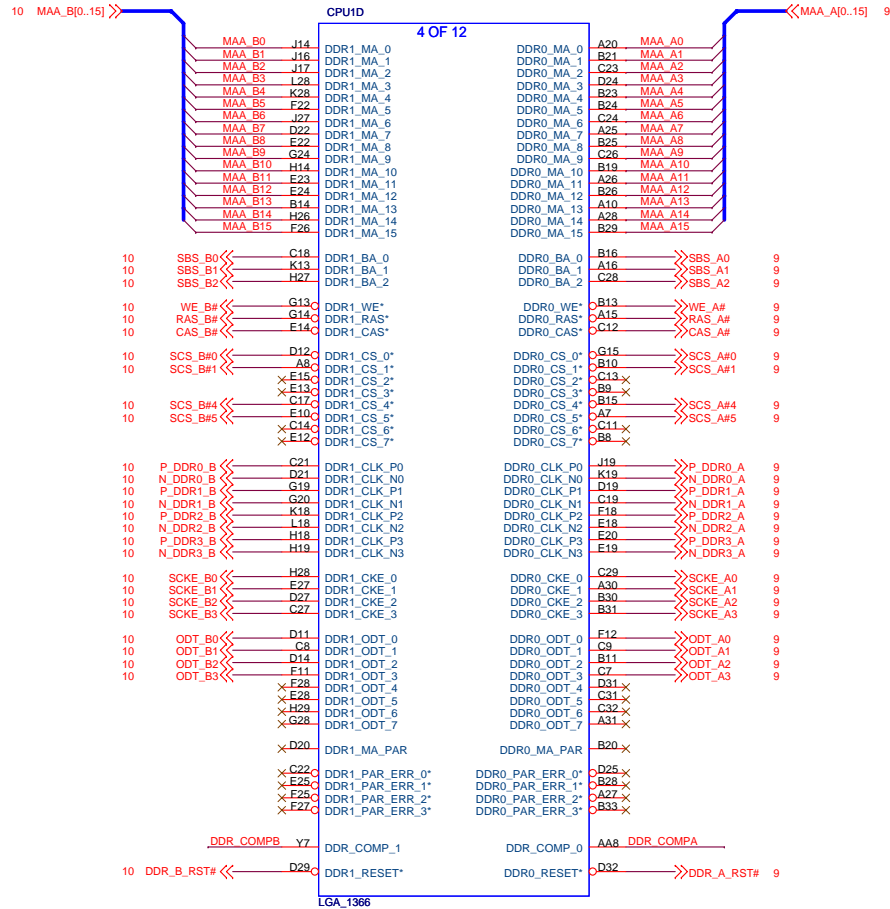
CPU1A 1 OF 12									
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DATA A4	W40	DDR0_DQ_3	DDR0_DQS_N1						
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DATA A9	N43	DDR0_DQ_9	DDR0_DQS_P3	B40	DQS_A#3	<<>	DQS_A#3	9	
DATA A10	K42	DDR0_DQ_10	DDR0_DQS_N3						
DATA A11	K43	DDR0_DQ_11		E3	DQS_A4	<<>	DQS_A4	9	
DATA A12	P42	DDR0_DQ_12	DDR0_DQS_P4	E4	DQS_A#4	<<>	DQS_A#4	9	
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DATA A31	B38	DDR0_DQ_31	DDR0_DQS_N10						
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DATA A33	C4	DDR0_DQ_33	DDR0_DQS_P11	G43		<<>			
DATA A34	F1	DDR0_DQ_34	DDR0_DQS_N11						
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DATA A49	N2	DDR0_DQ_49	DDR0_DQS_N16						
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DATA A51	T2	DDR0_DQ_51	DDR0_DQS_P17	B35		<<>			
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DATA A53	N3	DDR0_DQ_53							
DATA A54	R4	DDR0_DQ_54							
DATA A55	T3	DDR0_DQ_55							
DATA A56	U4	DDR0_DQ_56							
DATA A57	Y1	DDR0_DQ_57							
DATA A58	Y2	DDR0_DQ_58							
DATA A59	Y3	DDR0_DQ_59							
DATA A60	U1	DDR0_DQ_60							
DATA A61	U3	DDR0_DQ_61							
DATA A62	V4	DDR0_DQ_62							
DATA A63	W4	DDR0_DQ_63							
		DDR0_ECC_0		X36		<<>			
		DDR0_ECC_1		A36		<<>			
		DDR0_ECC_2		F32		<<>			
		DDR0_ECC_3		X33		<<>			
		DDR0_ECC_4		X37		<<>			
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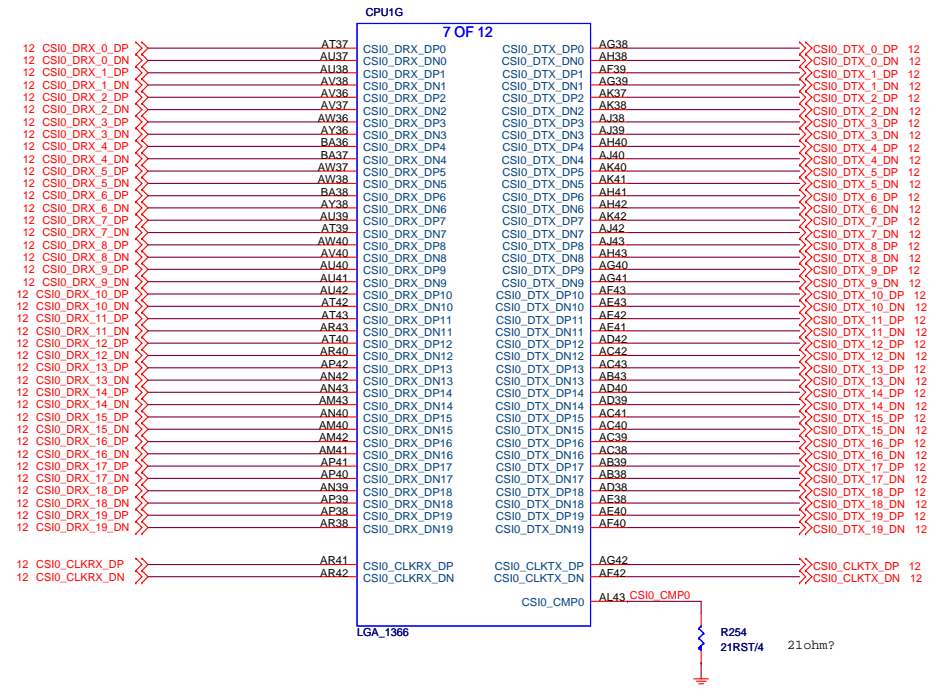
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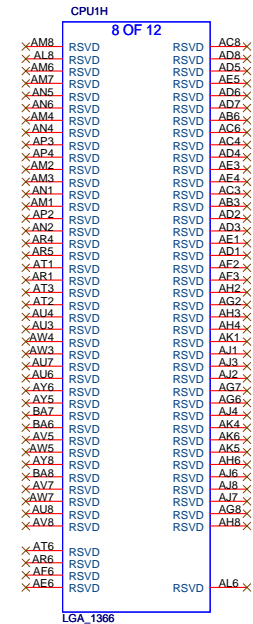
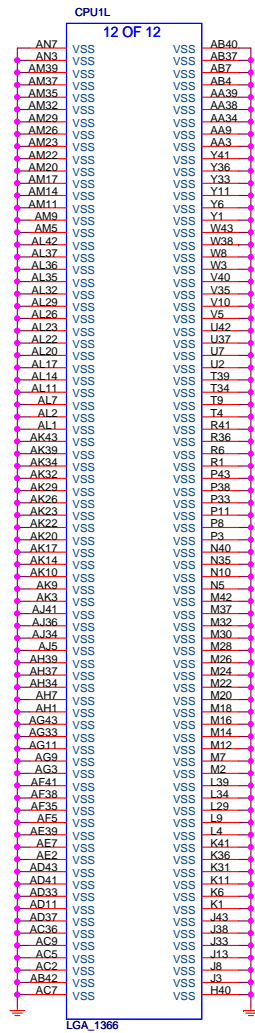
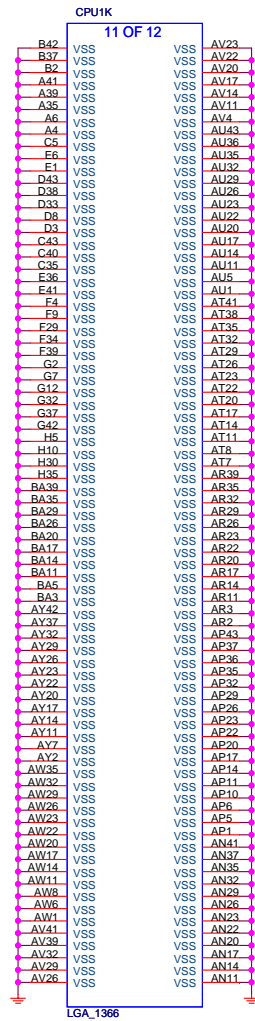
CPU1B 2 OF 12									
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DATA B1	AA36	DDR1_DQ_1	DDR1_DQS_N0	Y37	DQS_B#0	<<>	DQS_B#0	10	
DATA B2	Y36	DDR1_DQ_2							
DATA B3	Y34	DDR1_DQ_2	DDR1_DQS_P1	R38	DQS_B1	<<>	DQS_B1	10	
DATA B4	AA35	DDR1_DQ_3	DDR1_DQS_N1	R37	DQS_B#1	<<>	DQS_B#1	10	
DATA B5	AB36	DDR1_DQ_5							
DATA B6	Y40	DDR1_DQ_6	DDR1_DQS_P2	L35	DQS_B2	<<>	DQS_B2	10	
DATA B7	Y38	DDR1_DQ_7	DDR1_DQS_N2	L36	DQS_B#2	<<>	DQS_B#2	10	
DATA B8	P34	DDR1_DQ_9							
DATA B9	P35	DDR1_DQ_9	DDR1_DQS_P3	L30	DQS_B3	<<>	DQS_B3	10	
DATA B10	P38	DDR1_DQ_10	DDR1_DQS_N3	L31	DQS_B#3	<<>	DQS_B#3	10	
DATA B11	N38	DDR1_DQ_11							
DATA B12	R34	DDR1_DQ_12	DDR1_DQS_P4	E7	DQS_B4	<<>	DQS_B4	10	
DATA B13	R35	DDR1_DQ_13	DDR1_DQS_N4	D7	DQS_B#4	<<>	DQS_B#4	10	
DATA B14	N37	DDR1_DQ_14							
DATA B15	N38	DDR1_DQ_15	DDR1_DQS_P5	H6	DQS_B5	<<>	DQS_B5	10	
DATA B16	M35	DDR1_DQ_16	DDR1_DQS_N5	G6	DQS_B#5	<<>	DQS_B#5	10	
DATA B17	M34	DDR1_DQ_17							
DATA B18	K35	DDR1_DQ_18	DDR1_DQS_P6	L6	DQS_B6	<<>	DQS_B6	10	
DATA B19	J35	DDR1_DQ_19	DDR1_DQS_N6	L5	DQS_B#6	<<>	DQS_B#6	10	
DATA B20	N34	DDR1_DQ_20							
DATA B21	M36	DDR1_DQ_21	DDR1_DQS_P7	Y8	DQS_B7	<<>	DQS_B7	10	
DATA B22	J36	DDR1_DQ_22	DDR1_DQS_N7	Y9	DQS_B#7	<<>	DQS_B#7	10	
DATA B23	H36	DDR1_DQ_23							
DATA B24	H33	DDR1_DQ_24	DDR1_DQS_P8	G33		<<>			
DATA B25	L33	DDR1_DQ_25	DDR1_DQS_N8	G34		<<>			
DATA B26	K32	DDR1_DQ_26							
DATA B27	J32	DDR1_DQ_27	DDR1_DQS_P9	AA49		<<>			
DATA B28	J34	DDR1_DQ_28	DDR1_DQS_N9	AA44		<<>			
DATA B29	H34	DDR1_DQ_29							
DATA B30	L32	DDR1_DQ_30	DDR1_DQS_P10						
DATA B31	K30	DDR1_DQ_31	DDR1_DQS_N10						
DATA B32	E8	DDR1_DQ_32							
DATA B33	E8	DDR1_DQ_33	DDR1_DQS_P11	L37		<<>			
DATA B34	E5	DDR1_DQ_34	DDR1_DQS_N11	K37		<<>			
DATA B35	F5	DDR1_DQ_35							
DATA B36	F10	DDR1_DQ_36	DDR1_DQS_P12	K34		<<>			
DATA B37	G8	DDR1_DQ_37	DDR1_DQS_N12	K33		<<>			
DATA B38	D6	DDR1_DQ_38							
DATA B39	F6	DDR1_DQ_39	DDR1_DQS_P13	F8		<<>			
DATA B40	H8	DDR1_DQ_40	DDR1_DQS_N13	F7		<<>			
DATA B41	J6	DDR1_DQ_41							
DATA B42	G4	DDR1_DQ_42	DDR1_DQS_P14	H7		<<>			
DATA B43	H4	DDR1_DQ_43	DDR1_DQS_N14	J7		<<>			
DATA B44	G8	DDR1_DQ_44							
DATA B45	H8	DDR1_DQ_45	DDR1_DQS_P15	M5		<<>			
DATA B46	G5	DDR1_DQ_46	DDR1_DQS_N15	M4		<<>			
DATA B47	J5	DDR1_DQ_47							
DATA B48	K4	DDR1_DQ_48	DDR1_DQS_P16	Y4		<<>			
DATA B49	K5	DDR1_DQ_49	DDR1_DQS_N16	V5		<<>			
DATA B50	R5	DDR1_DQ_50							
DATA B51	T5	DDR1_DQ_51	DDR1_DQS_P17	F35		<<>			
DATA B52	J4	DDR1_DQ_52	DDR1_DQS_N17	F35		<<>			
DATA B53	M6	DDR1_DQ_53							
DATA B54	R8	DDR1_DQ_54							
DATA B55	R7	DDR1_DQ_55							
DATA B56	W6	DDR1_DQ_56							
DATA B57	W7	DDR1_DQ_57							
DATA B58	Y10	DDR1_DQ_58							
DATA B59	W10	DDR1_DQ_59							
DATA B60	V9	DDR1_DQ_60							
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DATA B63	W9	DDR1_DQ_63							
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		DDR1_ECC_4		E37		<<>			
		DDR1_ECC_5		E34		<<>			
		DDR1_ECC_6		X35		<<>			
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LGA_1366

CPU1C									
3 OF 12									
DATA C0	W34	DDR2_DQ_0	DDR2_DQS_P0	W37	DQS_C0	<<>	DQS_C0	11	
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DATA C2	V36	DDR2_DQ_2							
DATA C3	U36	DDR2_DQ_2	DDR2_DQS_P1	T37	DQS_C1	<<>	DQS_C1	11	
DATA C4	U34	DDR2_DQ_3	DDR2_DQS_N1	T38	DQS_C#1	<<>	DQS_C#1	11	
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DATA C7	V39	DDR2_DQ_7	DDR2_DQS_N2	K39	DQS_C#2	<<>	DQS_C#2	11	
DATA C8	U38	DDR2_DQ_9							
DATA C9	U39	DDR2_DQ_9	DDR2_DQS_P3	E39	DQS_C3	<<>	DQS_C3	11	
DATA C10	R39	DDR2_DQ_10	DDR2_DQS_N3	E40	DQS_C#3	<<>	DQS_C#3	11	
DATA C11	T36	DDR2_DQ_11							
DATA C12	W39	DDR2_DQ_12	DDR2_DQS_P4	J10	DQS_C4	<<>	DQS_C4	11	
DATA C13	V39	DDR2_DQ_13	DDR2_DQS_N4	J9	DQS_C#4	<<>	DQS_C#4	11	
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DATA C16	M39	DDR2_DQ_16	DDR2_DQS_N5	K7	DQS_C#5	<<>	DQS_C#5	11	
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DATA C19	J39	DDR2_DQ_19	DDR2_DQS_N6	P5	DQS_C#6	<<>	DQS_C#6	11	
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DATA C21	N36	DDR2_DQ_21	DDR2_DQS_P7	U8	DQS_C7	<<>	DQS_C7	11	
DATA C22	L40	DDR2_DQ_22	DDR2_DQS_N7	T8	DQS_C#7	<<>	DQS_C#7	11	
DATA C23	K38	DDR2_DQ_23							
DATA C24	G40	DDR2_DQ_24	DDR2_DQS_P8	G29	<<>				
DATA C25	F40	DDR2_DQ_25	DDR2_DQS_N8	G30	<<>				
DATA C26	J37	DDR2_DQ_26							
DATA C27	H37	DDR2_DQ_27	DDR2_DQS_P9	U35	<<>				
DATA C28	H39	DDR2_DQ_28	DDR2_DQS_N9	T35	<<>				
DATA C29	G39	DDR2_DQ_29							
DATA C30	F38	DDR2_DQ_30	DDR2_DQS_P10	U40	<<>				
DATA C31	E38	DDR2_DQ_31	DDR2_DQS_N10	T40	<<>				
DATA C32	K32	DDR2_DQ_32							
DATA C33	J12	DDR2_DQ_33	DDR2_DQS_P11	M38	<<>				
DATA C34	H13	DDR2_DQ_34	DDR2_DQS_N11	L38	<<>				
DATA C35	L13	DDR2_DQ_35							
DATA C36	G10	DDR2_DQ_36	DDR2_DQS_P12	H38	<<>				
DATA C37	G10	DDR2_DQ_37	DDR2_DQS_N12	G38	<<>				
DATA C38	H12	DDR2_DQ_38							
DATA C39	L12	DDR2_DQ_39	DDR2_DQS_P13	H11	<<>				
DATA C40	L10	DDR2_DQ_40	DDR2_DQS_N13	J11	<<>				
DATA C41	K10	DDR2_DQ_41							
DATA C42	M9	DDR2_DQ_42	DDR2_DQS_P14	K9	<<>				
DATA C43	N9	DDR2_DQ_43	DDR2_DQS_N14	K8	<<>				
DATA C44	L11	DDR2_DQ_44							
DATA C45	M10	DDR2_DQ_45	DDR2_DQS_P15	N4	<<>				
DATA C46	L18	DDR2_DQ_46	DDR2_DQS_N15	P4	<<>				
DATA C47	M6	DDR2_DQ_47							
DATA C48	P7	DDR2_DQ_48	DDR2_DQS_P16	V6	<<>				
DATA C49	N6	DDR2_DQ_49	DDR2_DQS_N16	J7	<<>				
DATA C50	P9	DDR2_DQ_50							
DATA C51	P10	DDR2_DQ_51	DDR2_DQS_P17	H31	<<>				
DATA C52	N7	DDR2_DQ_52	DDR2_DQS_N17	G31	<<>				
DATA C53	N9	DDR2_DQ_53							
DATA C54	R10	DDR2_DQ_54							
DATA C55	R9	DDR2_DQ_55							
DATA C56	U6	DDR2_DQ_56							
DATA C57	U6	DDR2_DQ_57							
DATA C58	T10	DDR2_DQ_58							
DATA C59	U10	DDR2_DQ_59							
DATA C60	T7	DDR2_DQ_60							
DATA C61	T7	DDR2_DQ_61							
DATA C62	V8	DDR2_DQ_62							
DATA C63	U9	DDR2_DQ_63							
	✗H32	DDR2_ECC_0							
	✗F33	DDR2_ECC_1							
	✗E29	DDR2_ECC_2							
	✗E30	DDR2_ECC_3							
	✗J31	DDR2_ECC_4							
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	✗F31	DDR2_ECC_6							
	✗F30	DDR2_ECC_7							







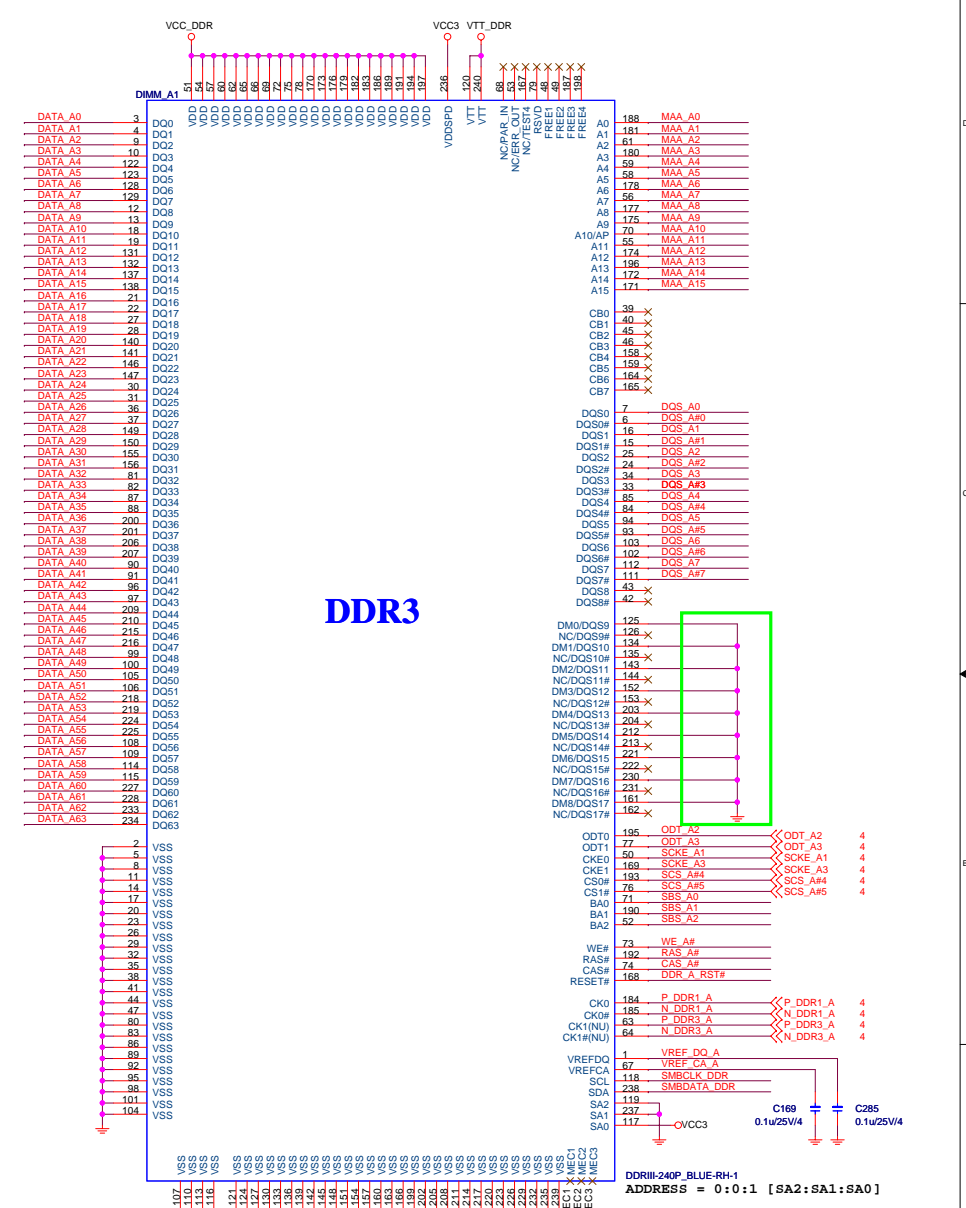
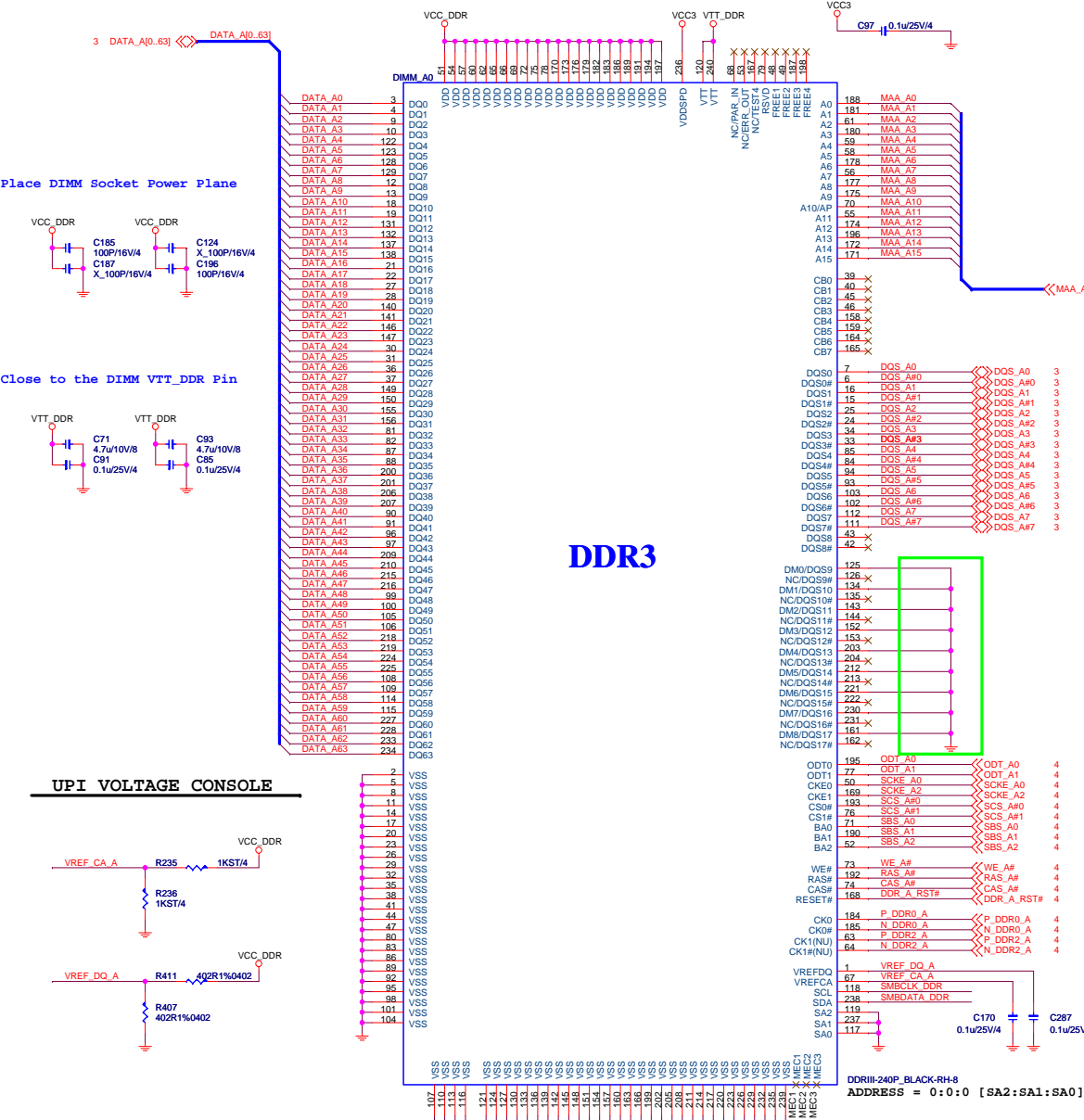
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MS-7522

Size Custom	Document Description LGA1366-GND	Rev 2.0
Date: Friday, October 24, 2008		Sheet 8 of 49

DIMM1 / CHANNEL A0

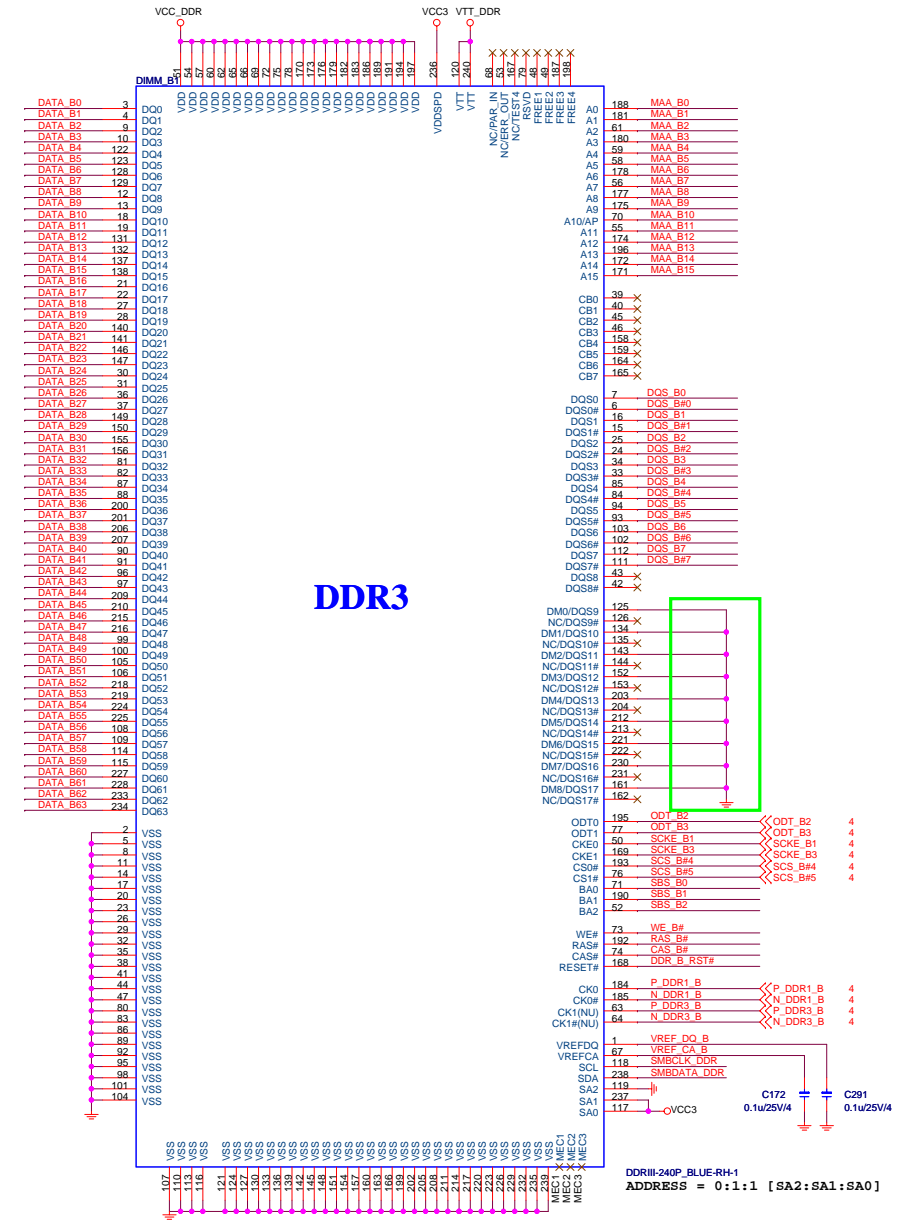
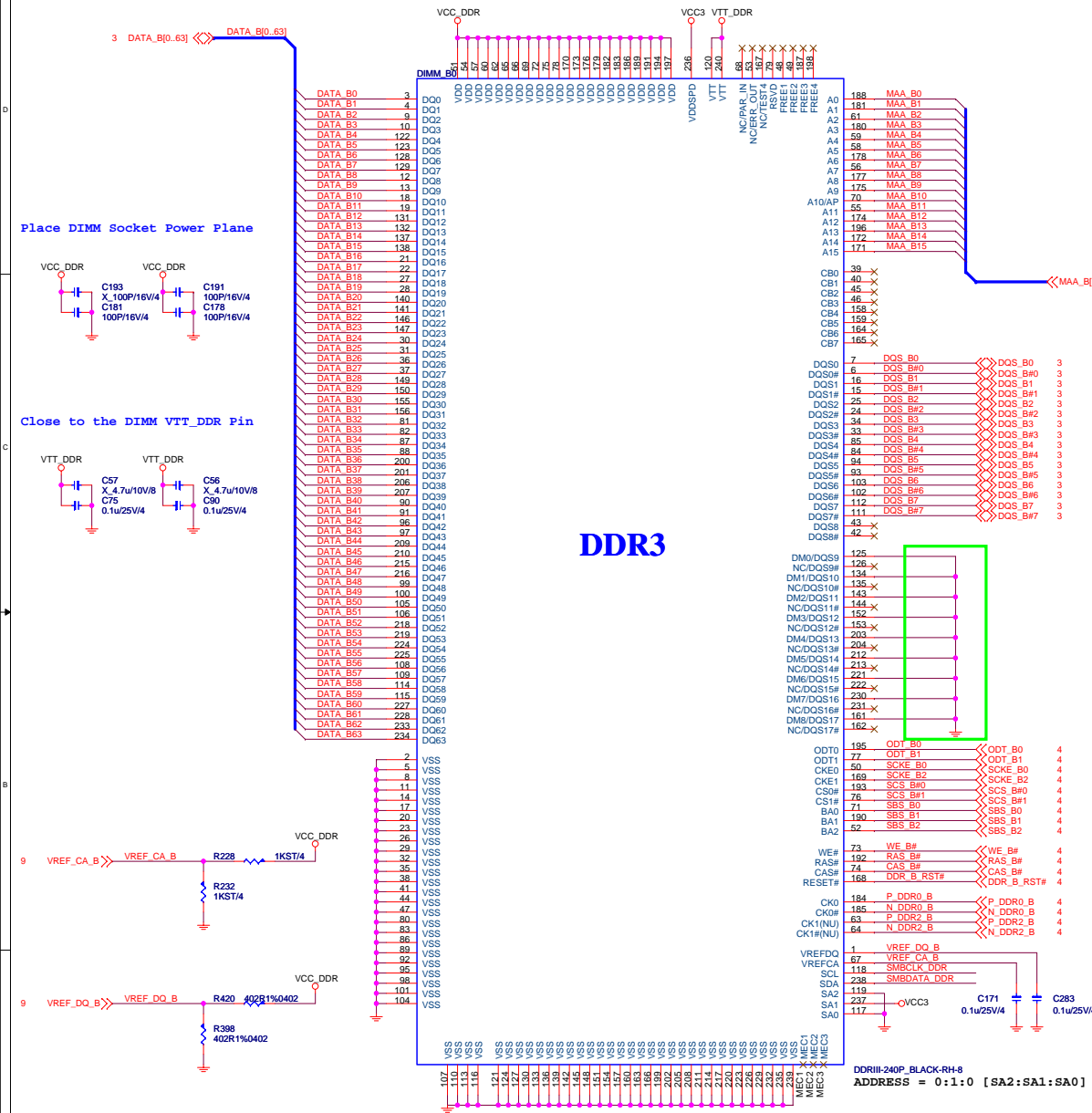
DIMM2 / CHANNEL A1



MICRO-STAR INT'L CO.,LTD		
MS-7522		
Size	Document Description	Rev
Custom	DDR III DIMM 1 / DIMM 2	2.0
Date: Tuesday, October 21, 2008	Sheet	9 of 49

DIMM3 / CHANNEL B0

DIMM4 / CHANNEL B1



Vref-DQ : Reference voltage for DQ0-DQ63, CB0-CB7 and PAR_IN. When in single ended mode used for DQS0-DQS7.

Vref-CA : Reference voltage for A0-A15, BA0-BA2, RAS#, CAS#, WE#, S0#, S01#, CKE0, CKE1, ODT0 and ODT1.

RESET#(Output) : A synchronously forces all registered output LOW when RESET# is LOW. This signal can be used during power up to ensure that CKE is LOW and DQs are High-Z.

SMBCLK_DDR << SMBCLK_DDR 9,11
SMBDATA_DDR << SMBDATA_DDR 9,11

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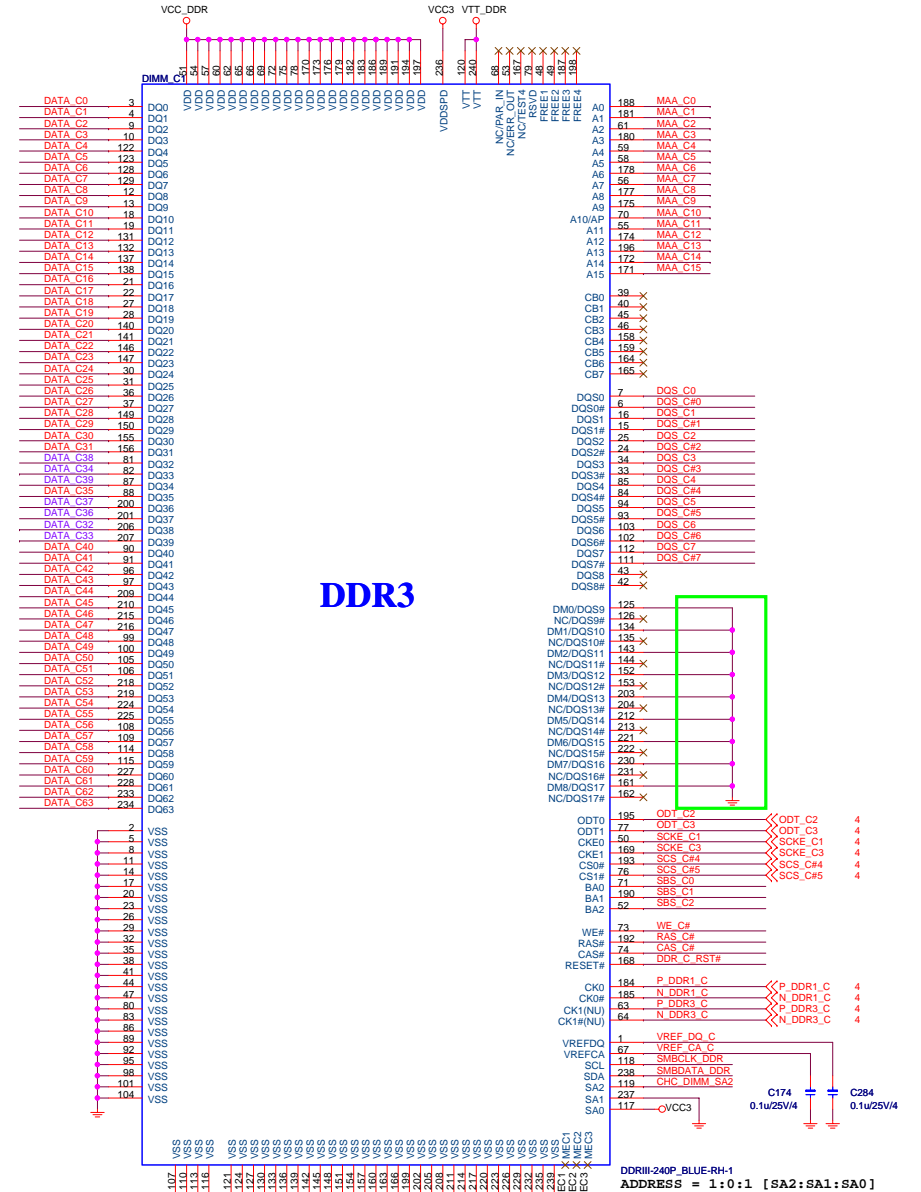
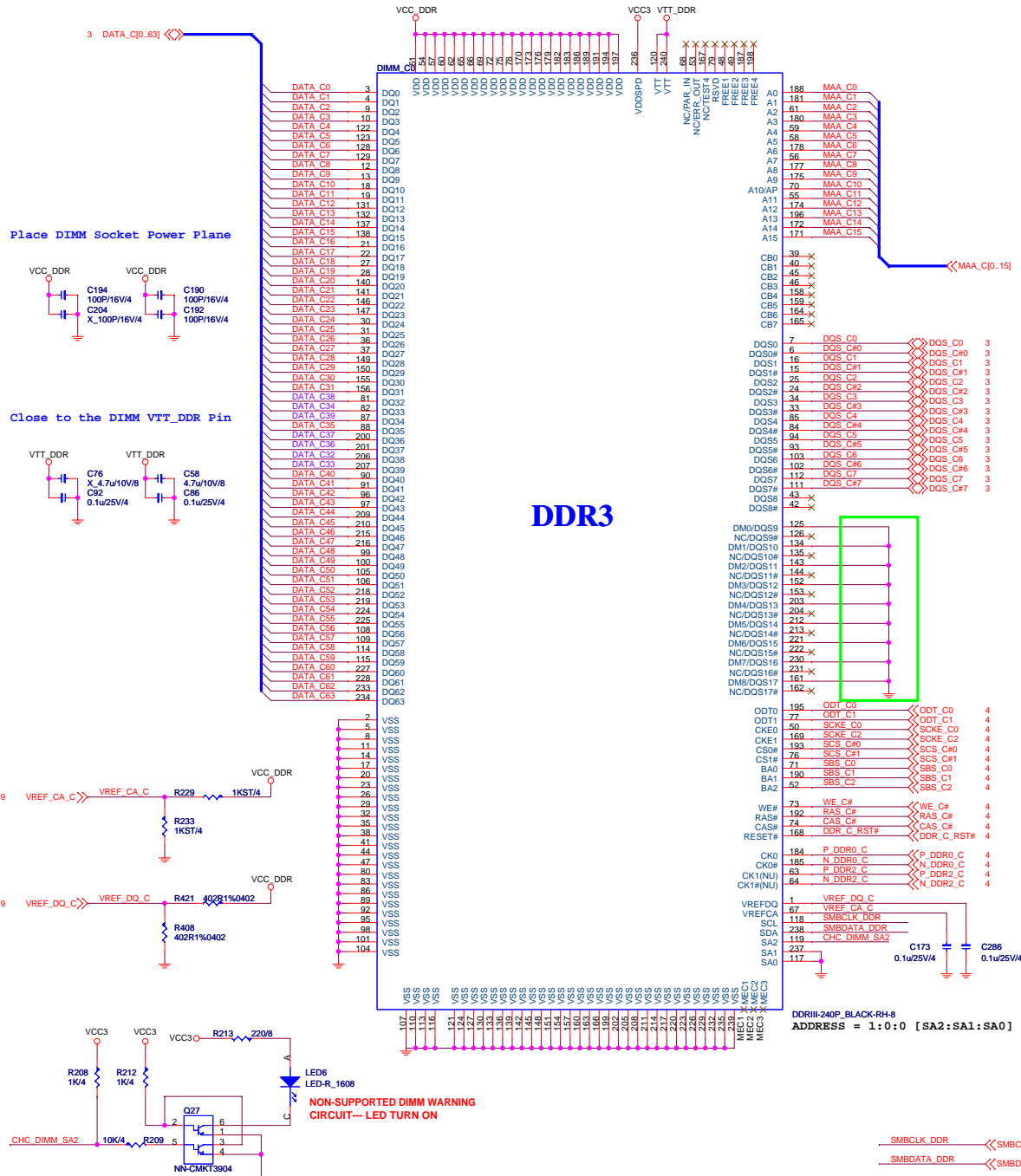
MS-7522

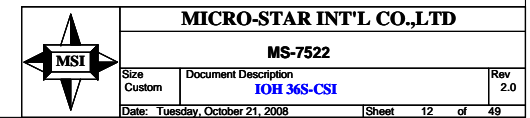
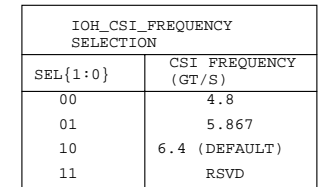
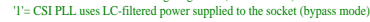
Size	Document Description	Rev
Custom	DDR III DIMM 3 / DIMM 4	2.0

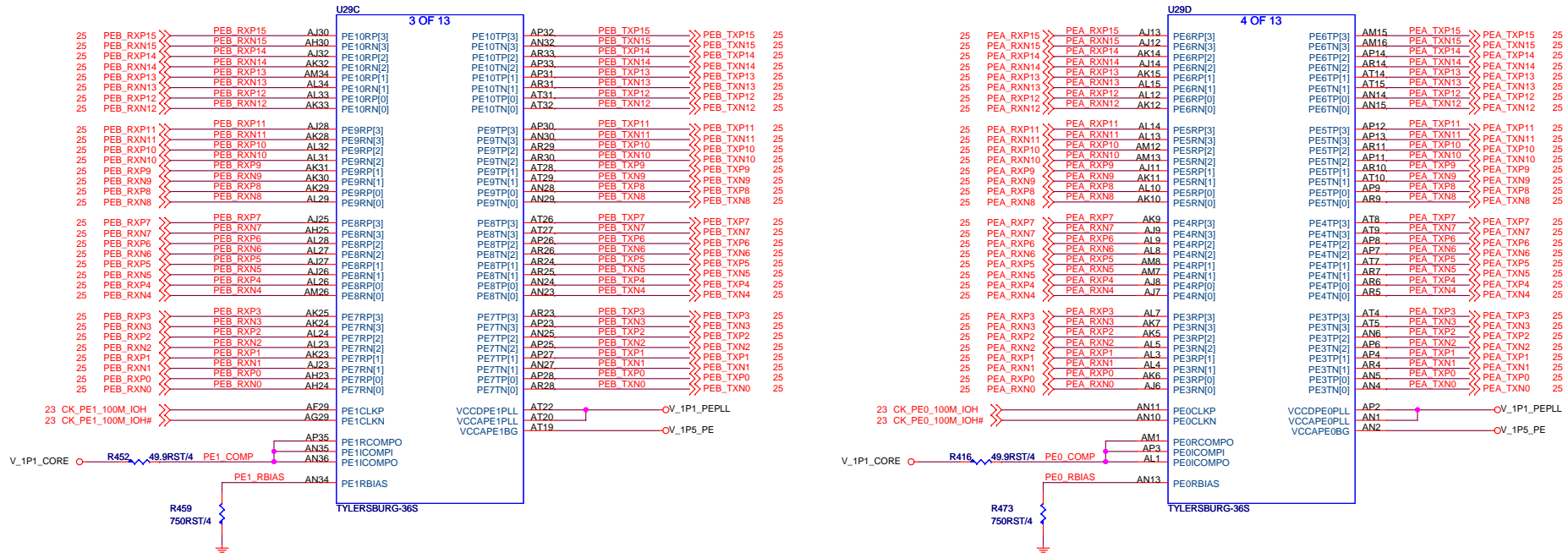
Date: Tuesday, October 21, 2008
Sheet 10 of 49

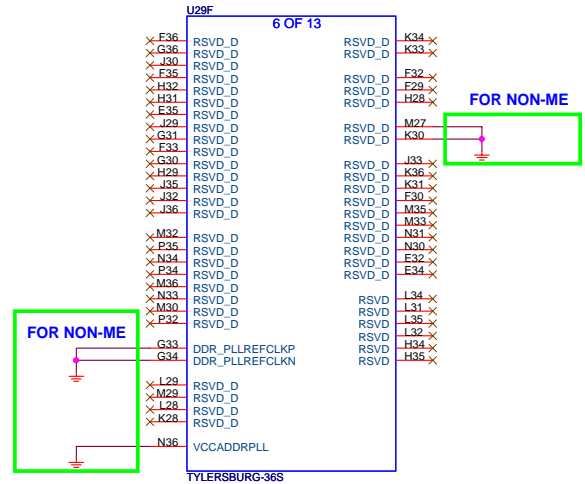
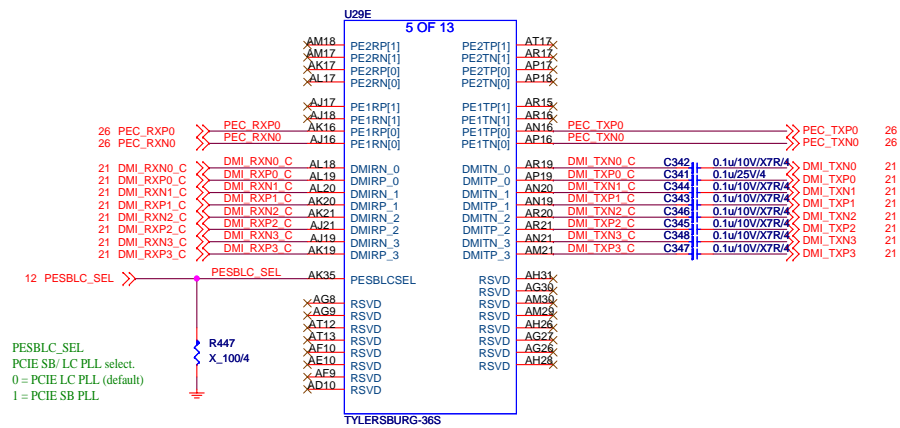
DIMM5 / CHANNEL C0

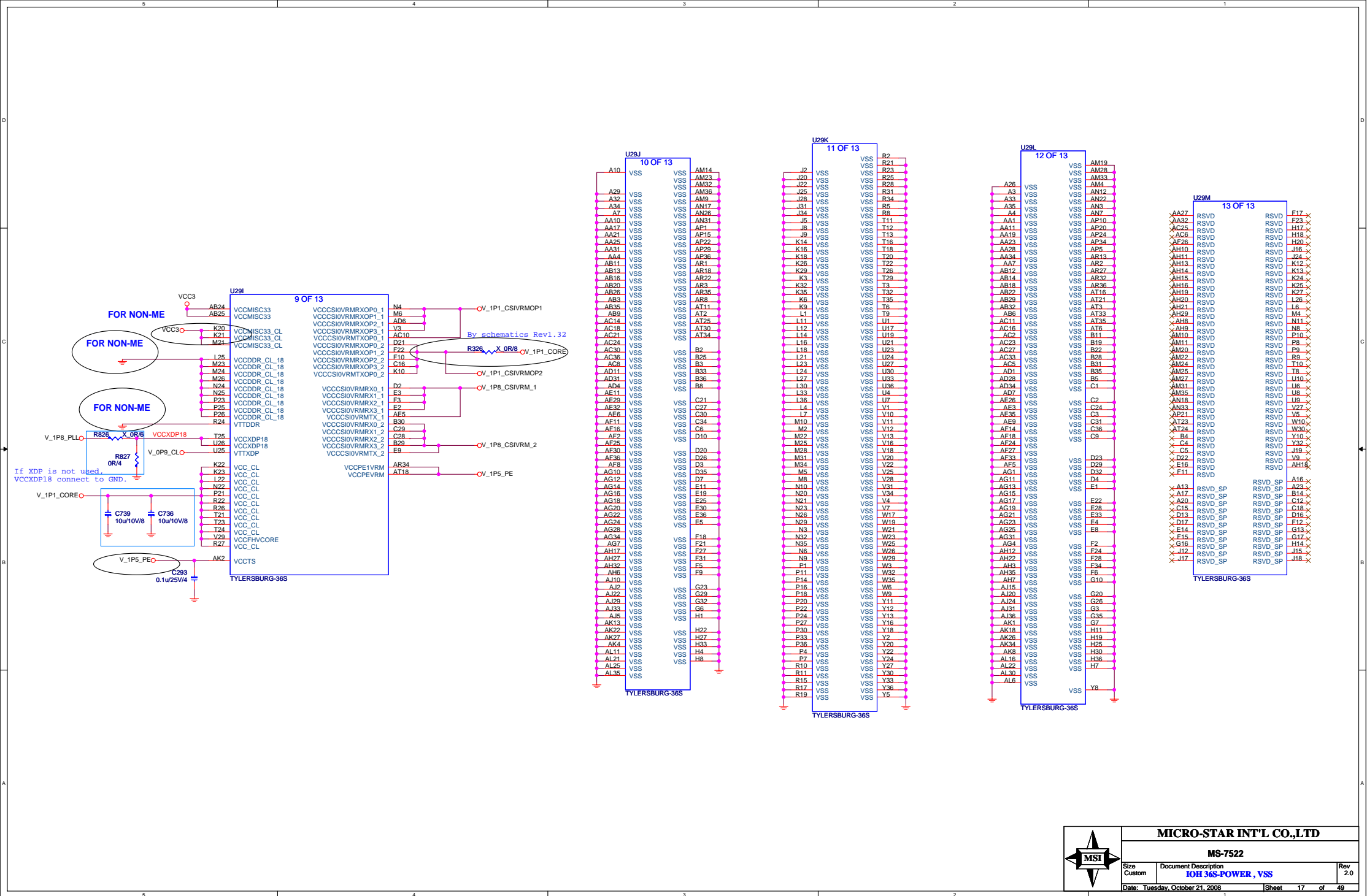
DIMM6 / CHANNEL C1









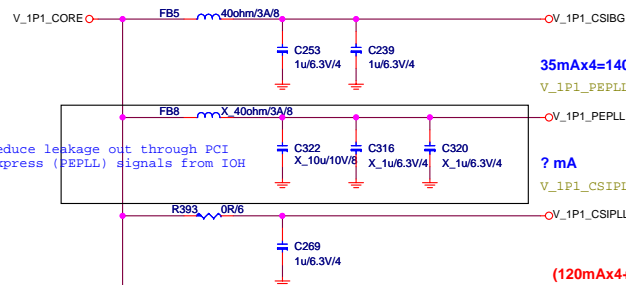


V_1P1_CORE REPLACE WITH V_1P1_VCCA

0.7A???

10mA \times 2=20mA

V_1P1_CSIBG = CSIBG_RX+CSIBG_TX



35mA \times 4=140mA

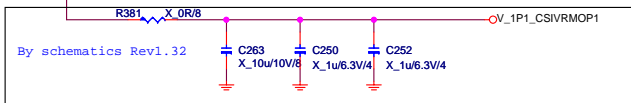
V_1P1_PEPLL = PEPLLA+PEPLLD

? mA

V_1P1_CSIPLL = CSI_PLL

(120mA \times 4+60mA)??=0.54A ?????

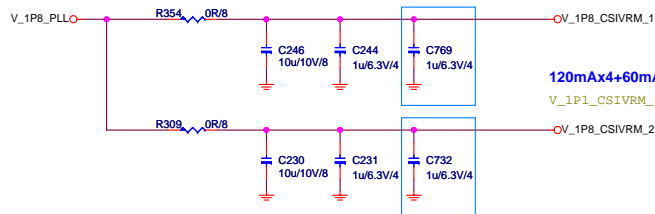
V_1P1_CSIVRMOP1 = CSIVRMOP_RX[1:4]+CSIVRMOP_TX1



1.08A

120mA \times 4+60mA=0.54A

V_1P1_CSIVRM_1 = CSIVRM_RX_1+CSIVRM1_TX_1



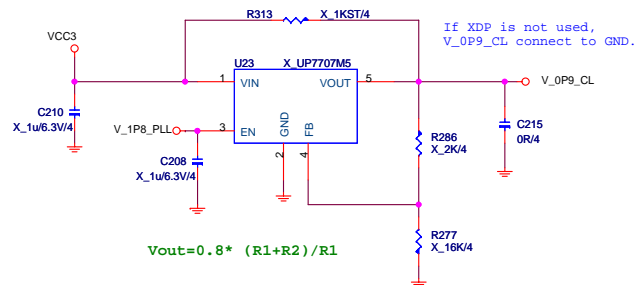
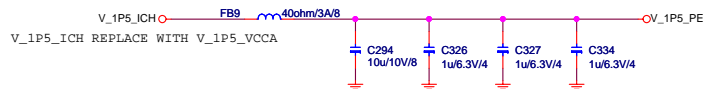
120mA \times 4+60mA=0.54A

V_1P1_CSIVRM_2 = CSIVRM_RX_2+CSIVRM1_TX_2

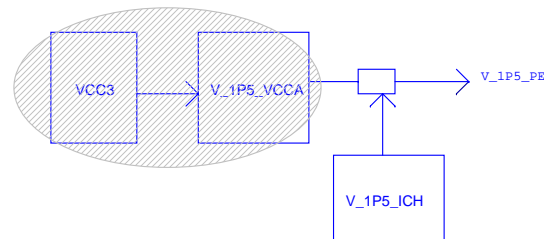
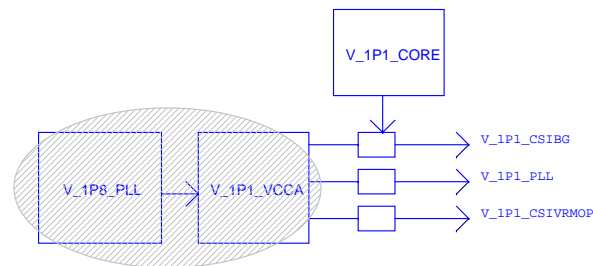
186.3mA+?

92mA \times 2+1.15mA \times 2+=186.3mA+?

V_1P5_PE = PEVRM+PEBG0+PEBG1+VCCTS



$$V_{out} = 0.8 \times (R1 + R2) / R1$$

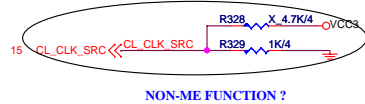
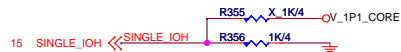
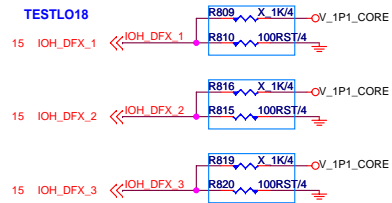
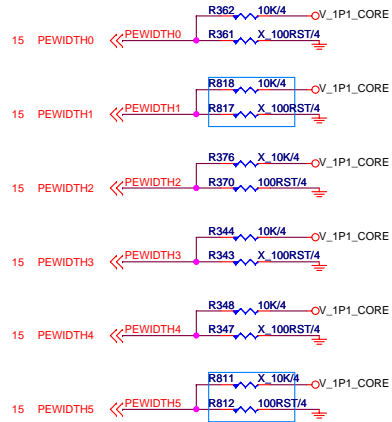


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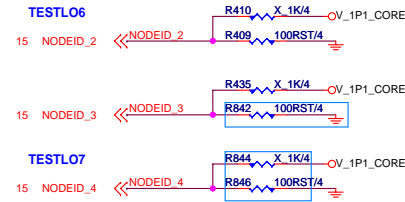
MS-7522

Size	Document Description	Rev
Custom	IOH 365-ANALOG FILTER	2.0
Date:	Tuesday, October 21, 2008	Sheet 18 of 49

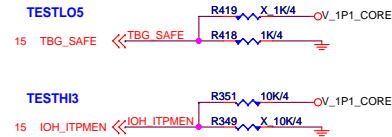
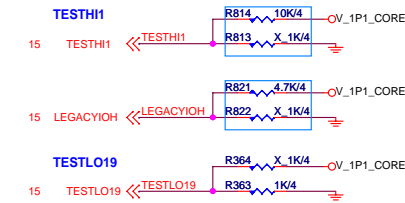
PEWIDTH0~5
PCIE Link Width Select
"110110" X2, X2, X16, X16
"111011" = 2x16
"101111" = 4x8
"011111" = Wait On Bios



NODEID_3_TBG
For dual TBG IOH configuration,
it indicates which CSI port is connected
to the other IOH.
"0": CSI0
"1": CSI1



LEGACYIOH
Used to determine legacy or non-legacy selection:
"1": Legacy IOH
"0": Non-legacy IOH



IOH_DFX_[2 , 3]
DDR frequency selection pins:
DDRFRQ[3:2] as DDR frequency selection defined as:
"00" = 133MHz input, 200MHz core
"01" = 100 MHz input, 200MHz core
"10" = RSVD
"11" = RSVD

SINGLE_IOH
Used for dual TBG IOH selection:
"0": IOH is not connected to another IOH on some CSI link (default)
"1": IOH is connected to another IOH on some CSI link

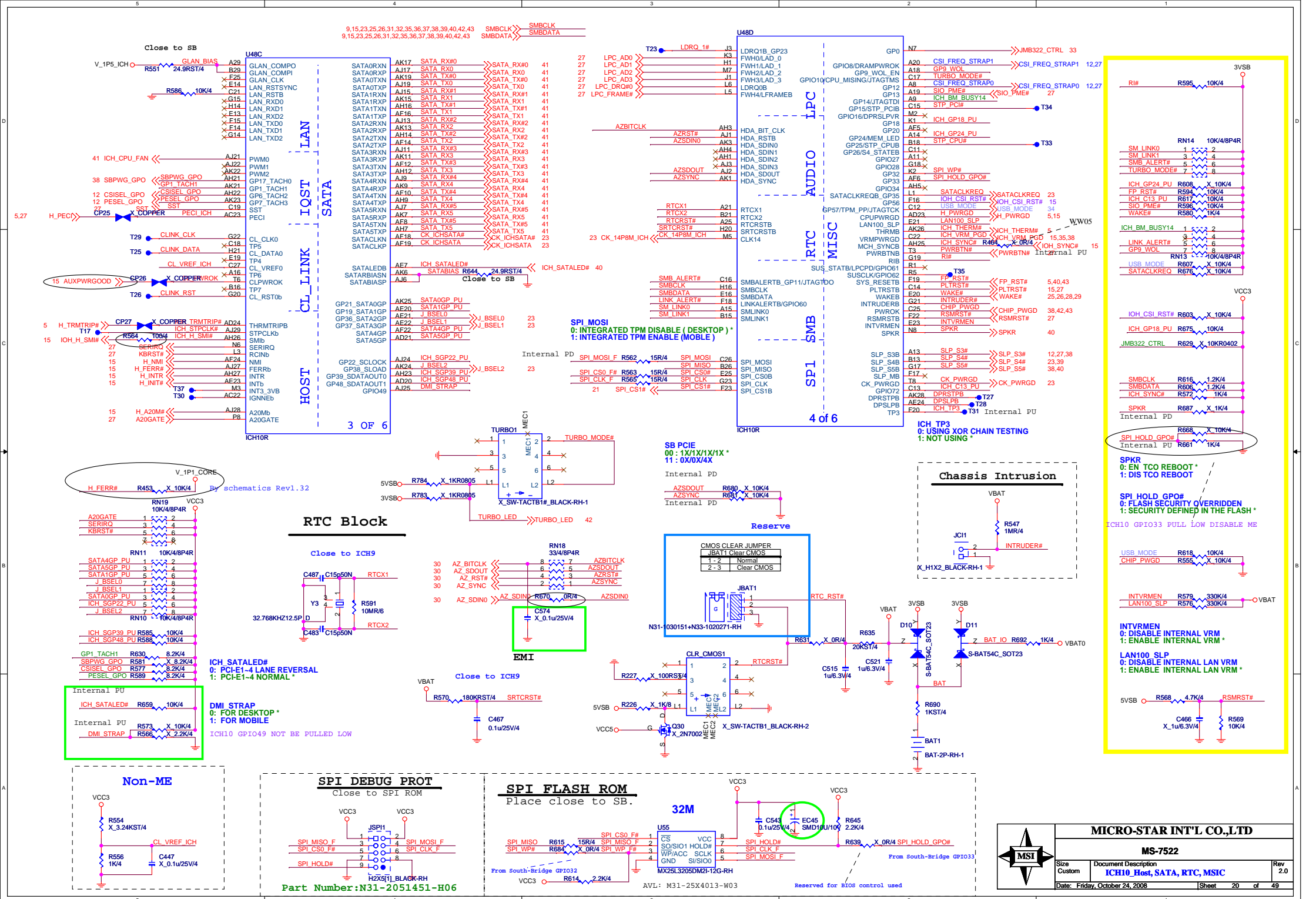
CL_CLK_SRC
Used for ME default clock source:
"1": PLL (default)
"0": Ring Oscillator (back-up)

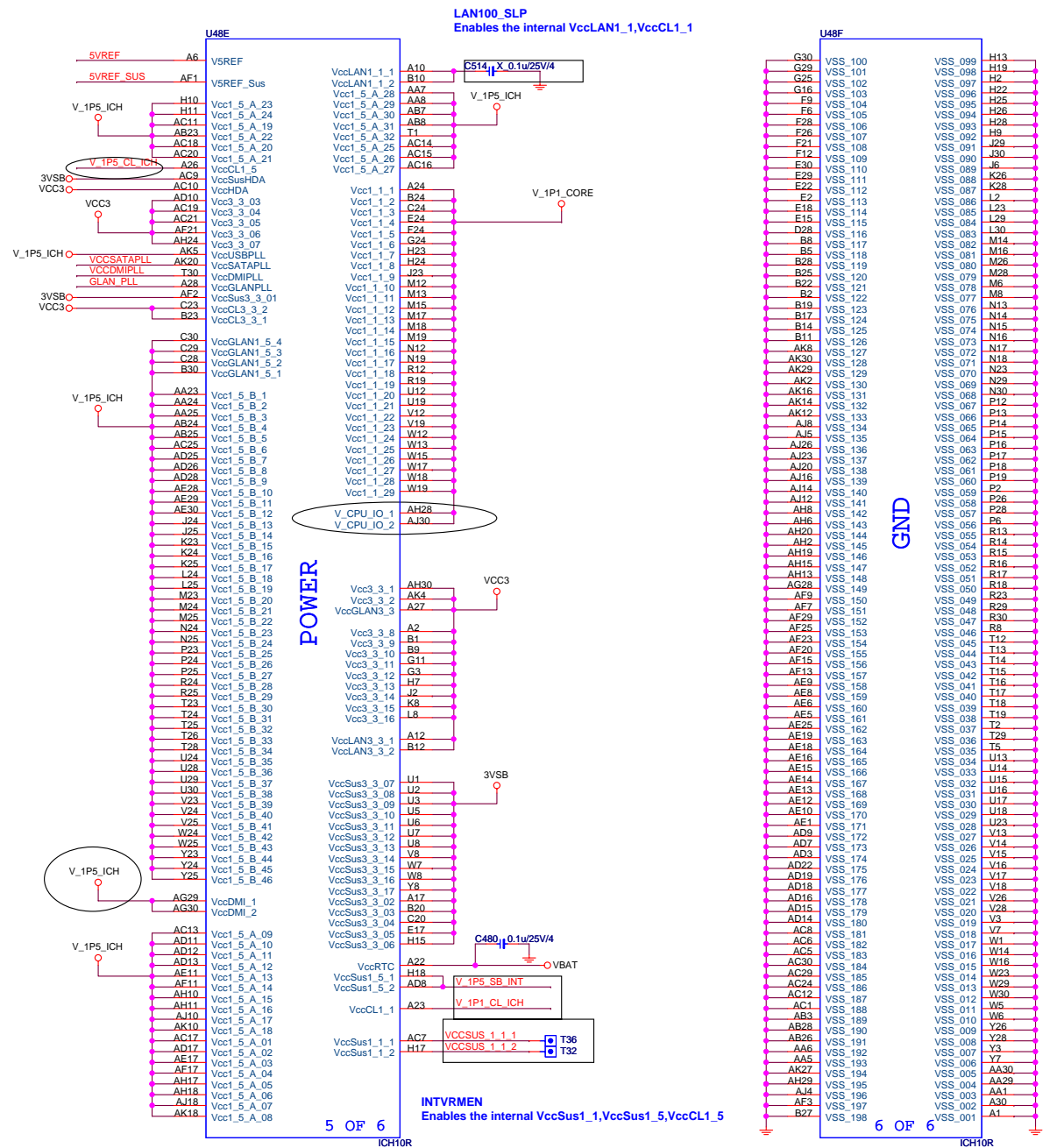


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MS-7522

Size Custom	Document Description IOH 36S-STRAP	Rev 2.0
Date: Tuesday, October 21, 2008	Sheet 19 of 49	

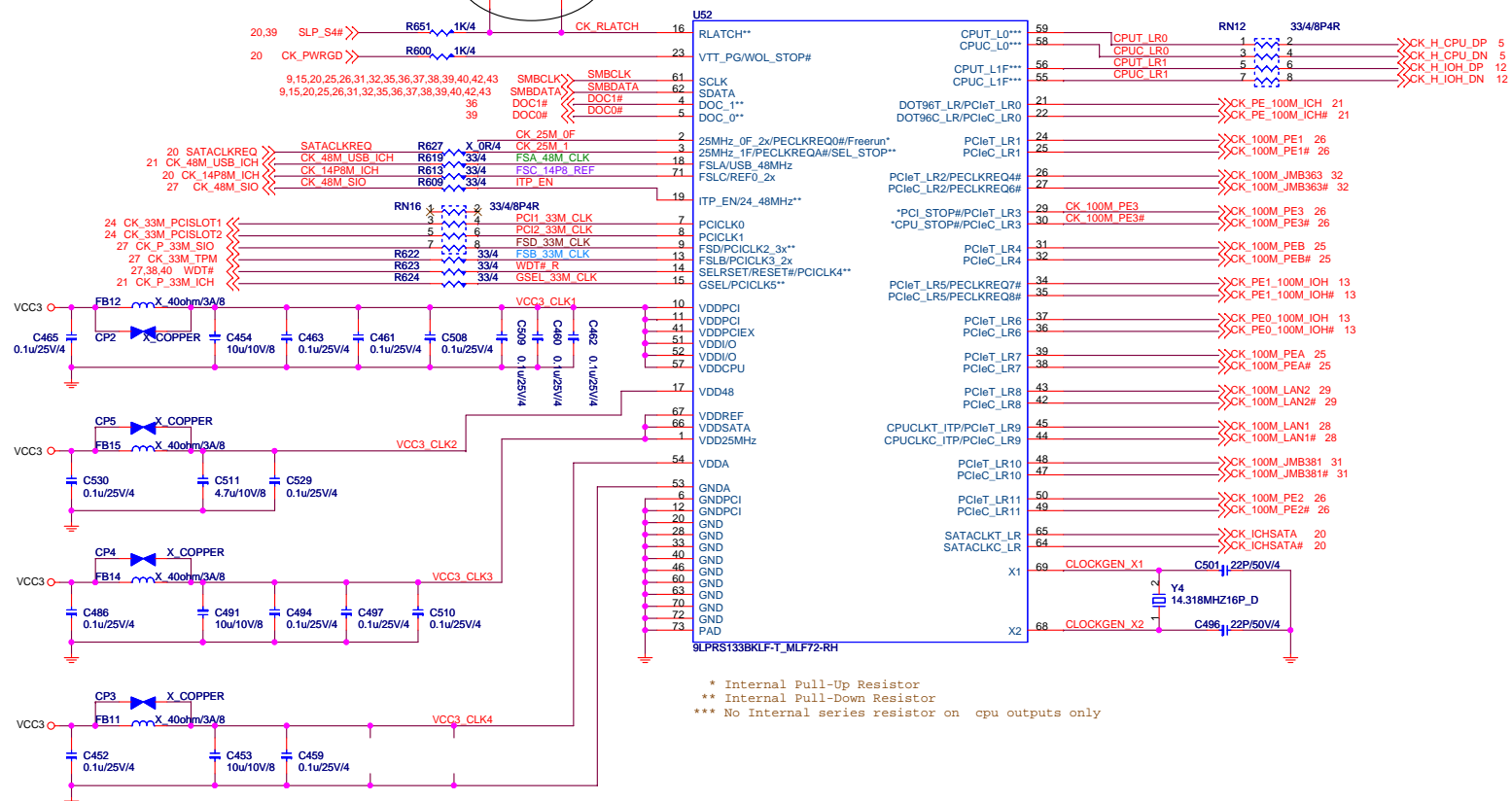




MS-7522

Size Custom	Document Description ICH10_Power, GND	Rev 2.0
Date: Tuesday, October 21, 2008		Sheet 22 of 49

Clock Gen ICS9LPRS133



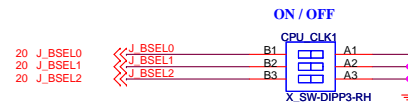
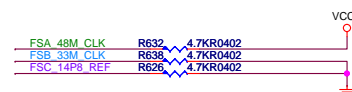
Default 0 0 1 133 MHz

JB3 1-2 PIN 1

JB2 2-3 PIN 0

JB1 2-3 PIN 0

BSEL			TABLE
2	1	0	FSB FREQUENCY
0	0	0	266 MHz
0	0	1	133 MHz (default)
0	1	0	200 MHz
0	1	1	166 MHz
1	0	0	333 MHz
1	0	1	100 MHz
1	1	0	400 MHz
1	1	1	200 MHz



CLOCK GEN STRAPING

0 : Pin21/22 100MHz * **GSEL 33M CLK** **R649** **4.7K/4**
1 : Pin21/22 96MHz Internal pull down

0: PCICLK4
1: RESET* WDT# R R648 4.7K/4 VCC3

0: PCIEX9 * ITP_EN R610 4.7K/4
1: CPU ITP Internal pull down

1 : 25MHz freerun function

CK_25M_0F

R646 X 4.7K/4

R636 X 4.7K/4

VCC3

Internal pull up

1 = Selects pin 29/30 to be PCI_STOP#/CPU_STOP#

0 = Selects pin 29/30 to be PCI_E_CLK

CK_25M_1 R647 4.7K/4
Internal pull down

For ICS CPU/DIV SEL
0 = FSLD BIT2 = 0 *

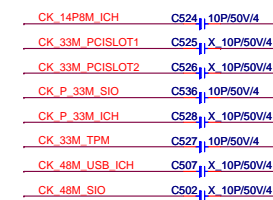
For ICS CPU/DIV SEL
0 = FSLD BIT2 = 0 *

0: FSLD BIT3=0
1: FSLD BIT3=1

FSD_33M_CLK R637 4.7K/4
Internal pull up

0: FSLD BIT3=0
1: FSLD BIT3=1

FSD_33M_CLK R637 4.7K/4
Internal pull up



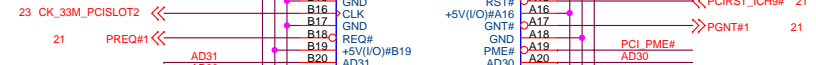
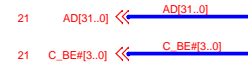
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MS-7522

Size Custom	Document Description Clock Gen ICS9LPRS133	Rev 2.0
Date: Tuesday, October 21, 2008		Sheet 23 of 49

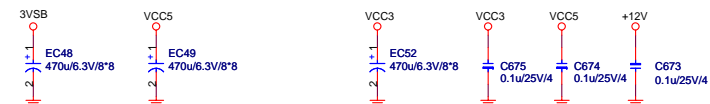
Rev
2.0

PCI SLOT 2 (PCI VER: 2.2 COMPLY)



```
IDSEL = AD17
MASTER = PREQ#1
PGNT#1
```

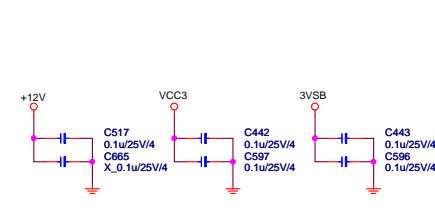
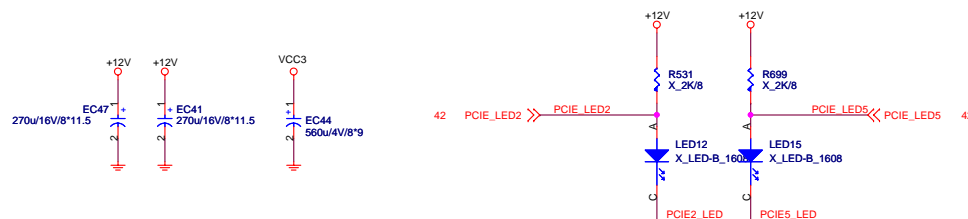
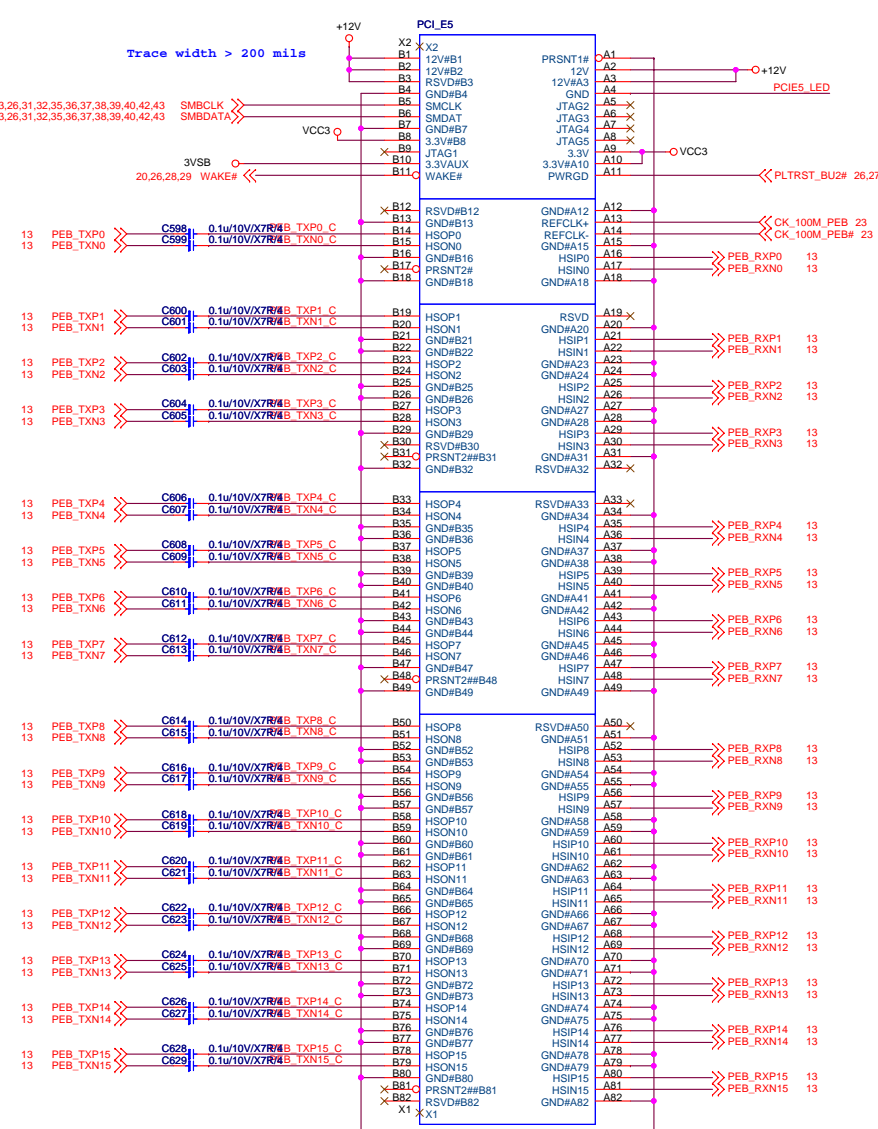
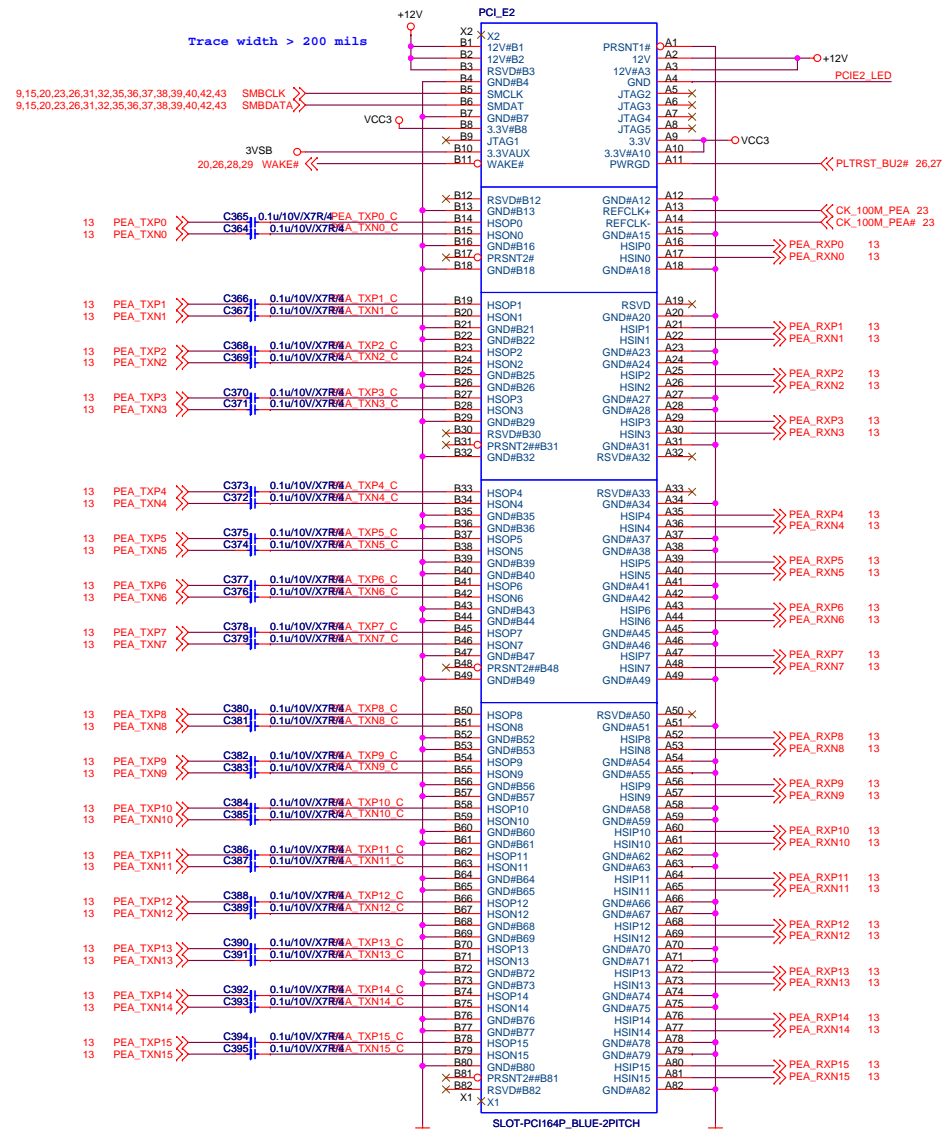
Figure 10: Pin connections for the internal PU. The diagram shows two main sections: the top section for VCC3 and the bottom section for 3VSB. The VCC3 section includes signals like DEVSEL#, TRDY#, IRDY#, FRAME#, SERR#, PERR#, LOCK#, STOP#, REQ#64, ACK#64, and internal PU signals R767, R768, and R740. The 3VSB section includes signals like PREQ#0, PREQ#1, PREQ#2, PREQ#3, PIQ#C, PIQ#D, PIQ#B, PIQ#A, and internal PU signals R770, R833, R621, R674, and R740. The diagram also shows connections to VCC3 and 3VSB pins.



MS-7522

Size Custom	Document Description PCI SLOT1 , 2	Rev 2.0
Date: Tuesday, October 21, 2008		Sheet 24 of 49

PCI_Express X16 SLOT1,2



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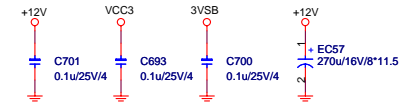
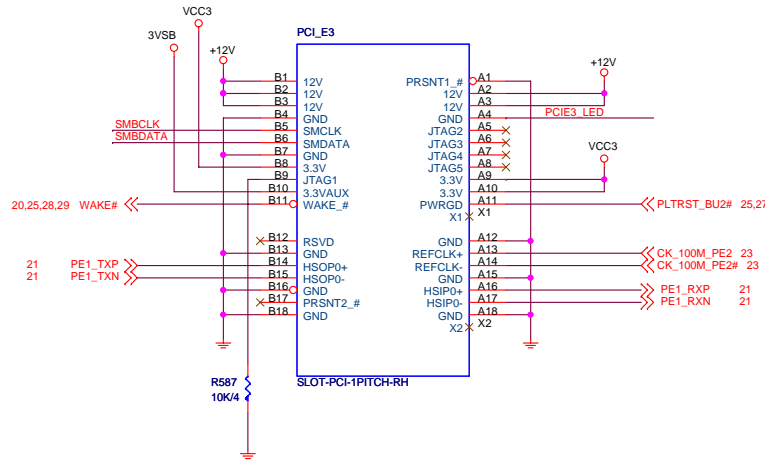
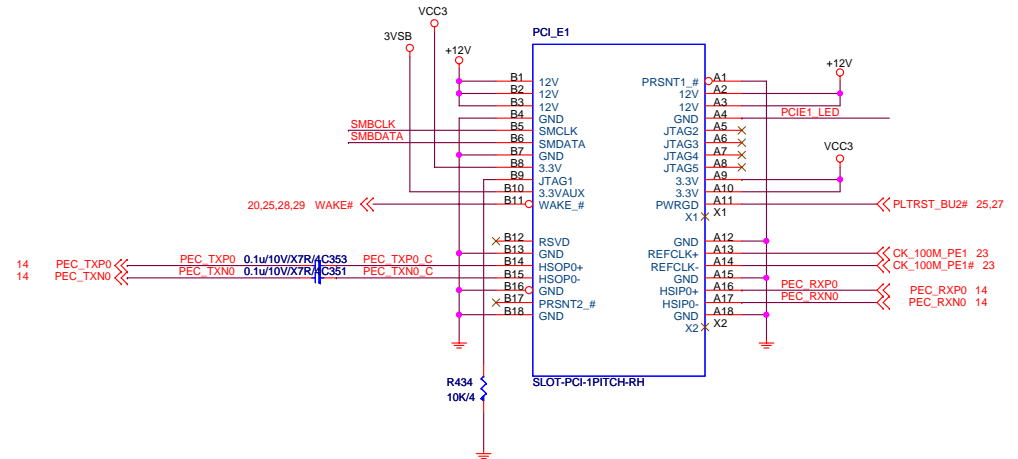
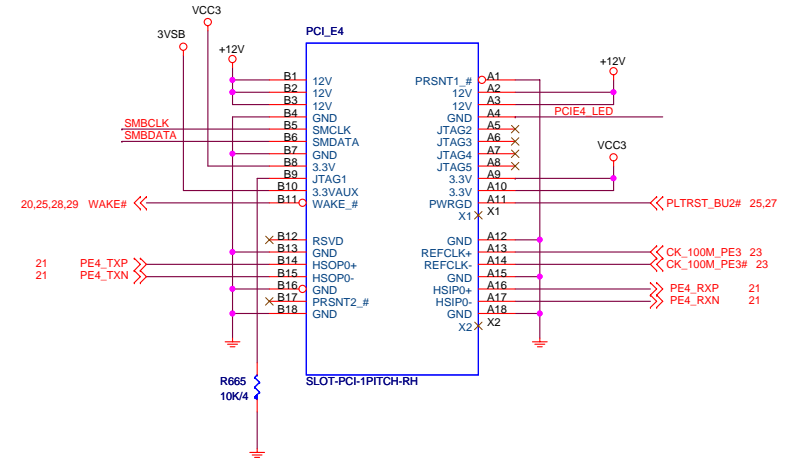
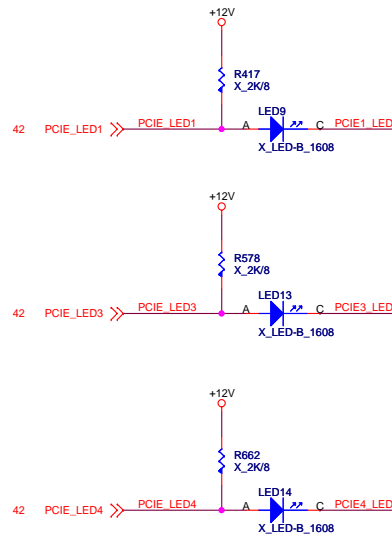
MS-7522

Size Custom	Document Description PCI-E X16 SLOT1, 2	Rev 2.0
Date: Tuesday, October 21, 2008		Sheet 25 of 49

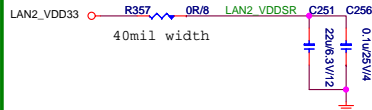
PCI_Express X1 Slot1 , 2 , 3

Trace width > 200mils

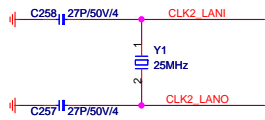
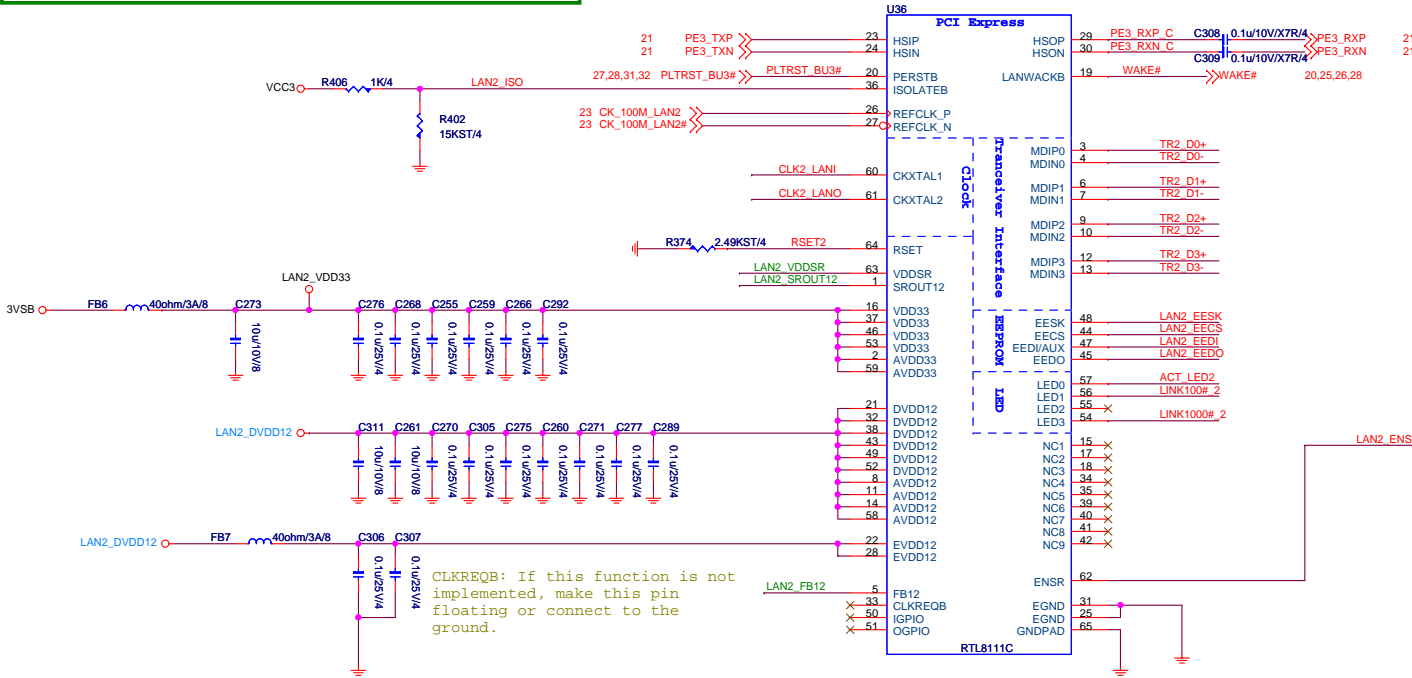
9,15,20,23,25,31,32,35,36,37,38,39,40,42,43 SMBCLK
9,15,20,23,25,31,32,35,36,37,38,39,40,42,43 SMBDATA



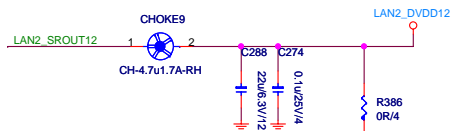
For the power pin of the switching regulator,
Disable switching regulator: Remove R27, C20, C21



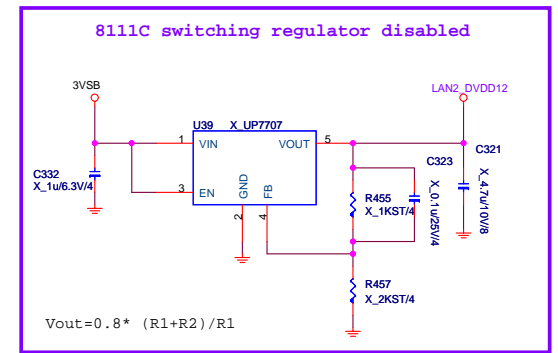
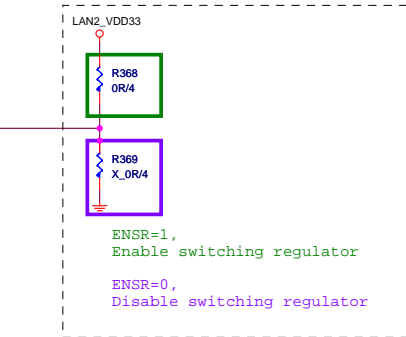
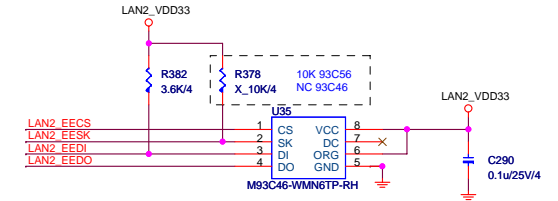
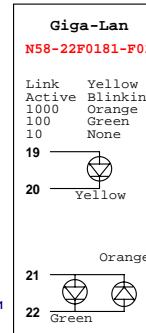
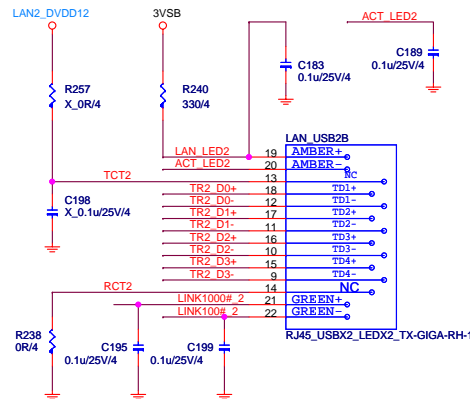
C657 C346 near Pin63 200mil, C346 must be nearly Pin63

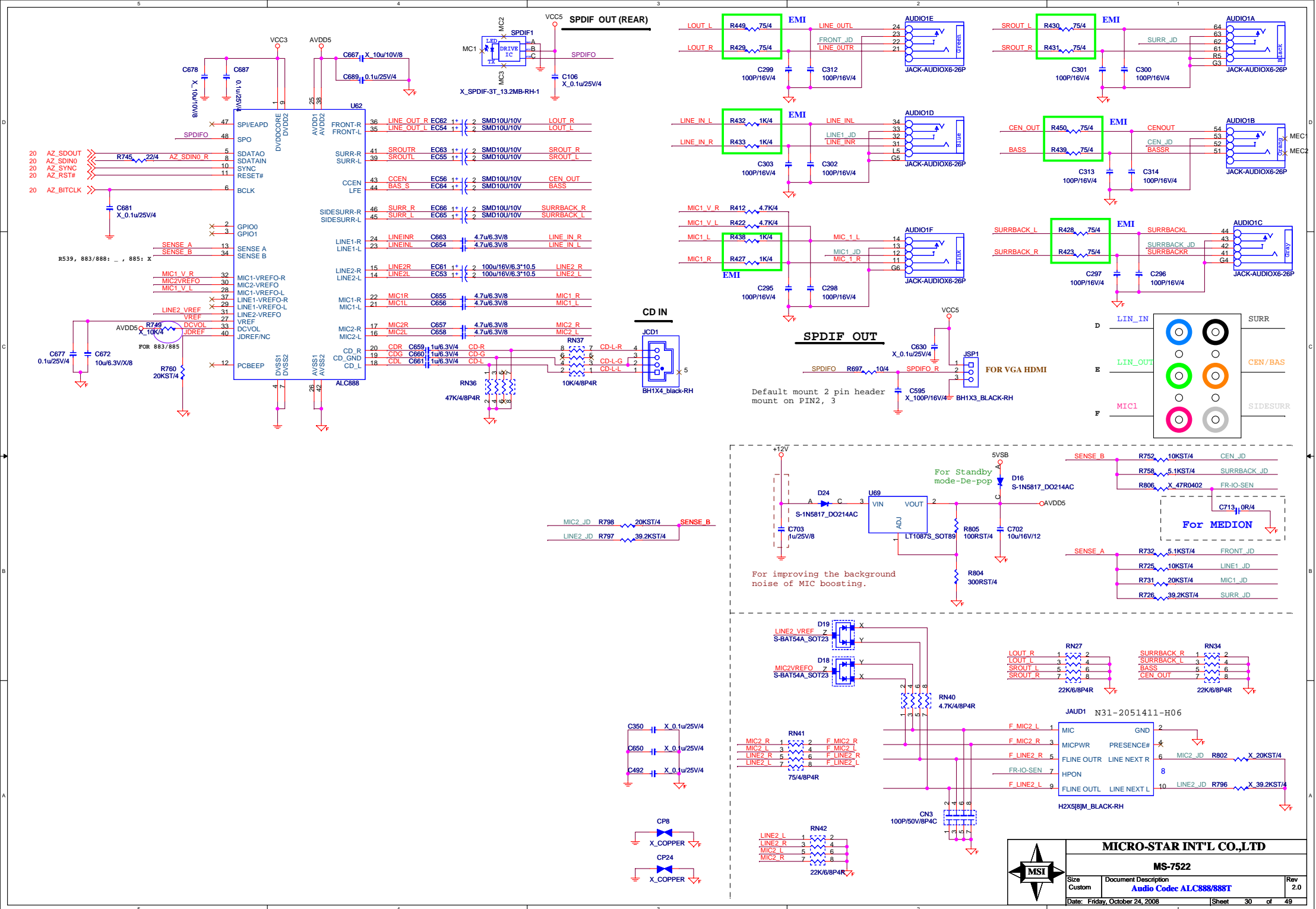


Choke C656 C345 near Pin1 200mil

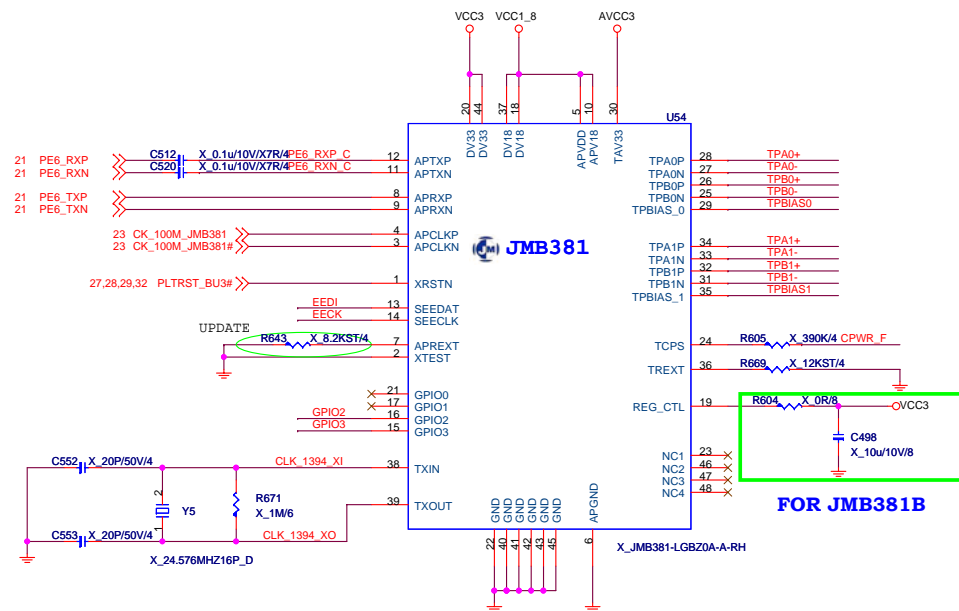


"FB12": A trace front CHOKE to RTL8111C pin5

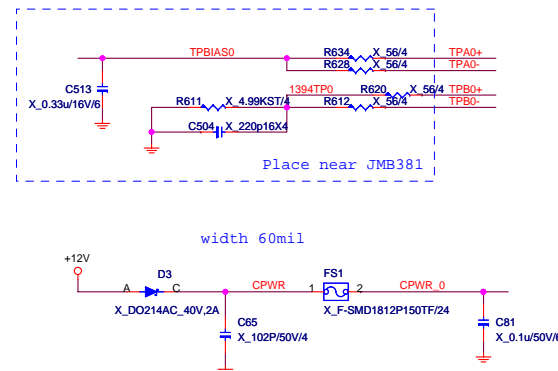




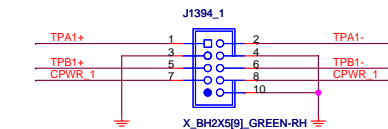
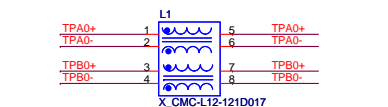
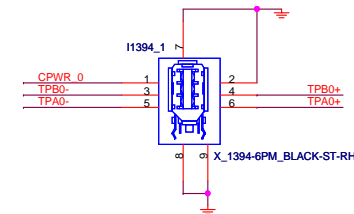
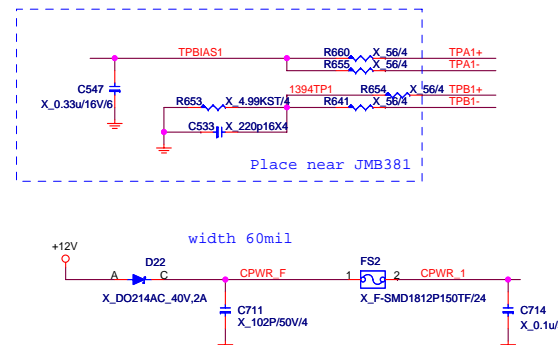
1394 CONTROLLER



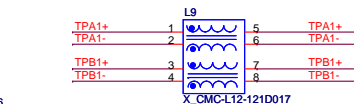
Rear 1394 port



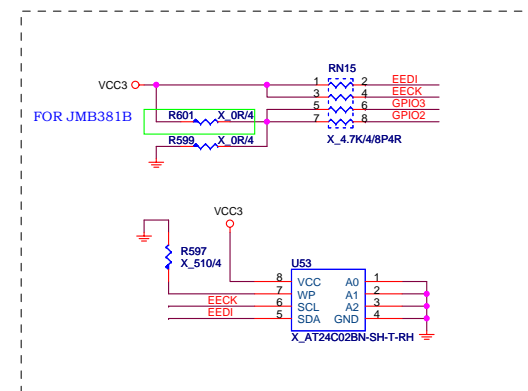
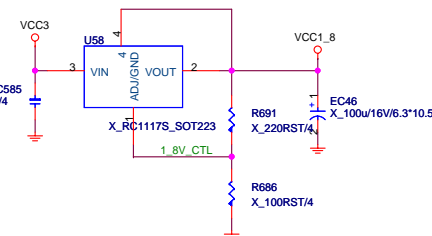
Front 1394 pin header

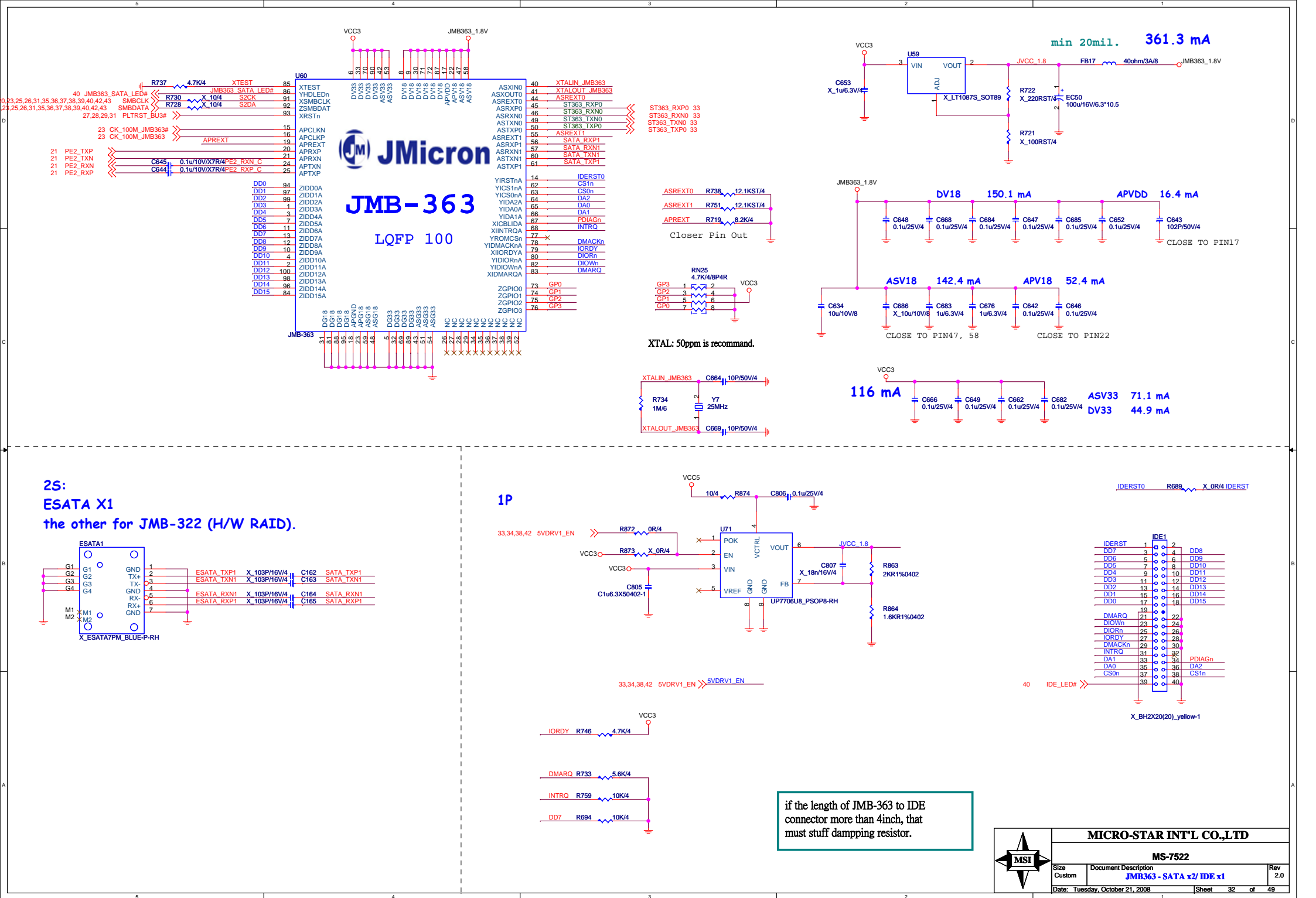


For Intel 1394 pinheader

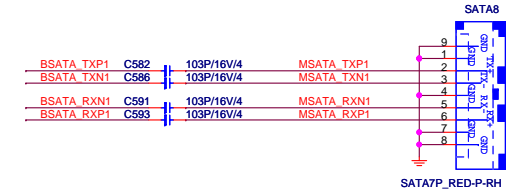
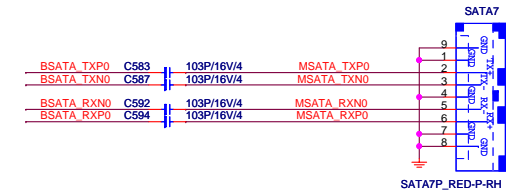
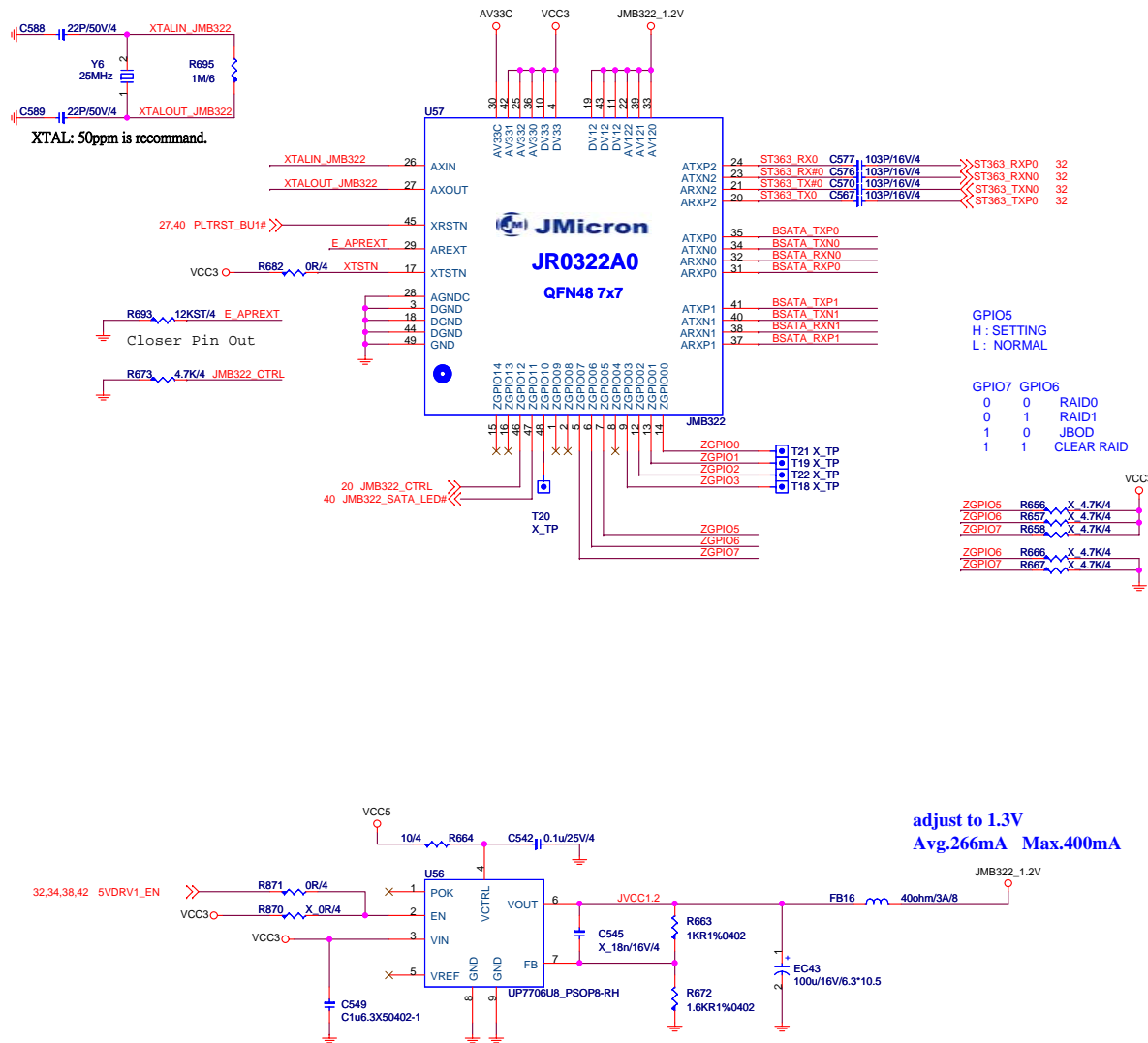


A1117 CO-LAY SOT223 (TO_261) PNP BJT





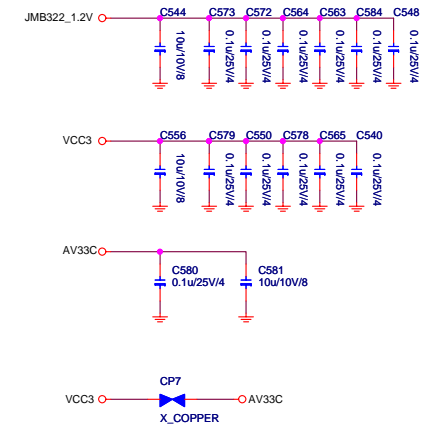
JMB322 - H/W RAID CONTROLLER



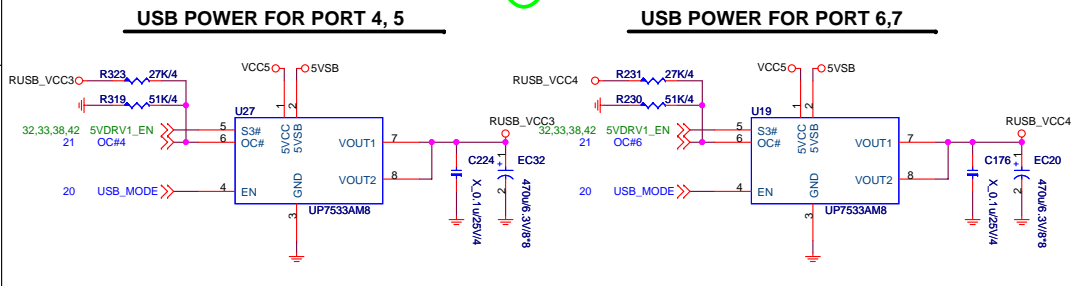
GPIO5
H: SETTING
L: NORMAL

GPIO7 GPIO6
0 0 RAID0
0 1 RAID1
1 0 JBOD
1 1 CLEAR RAID

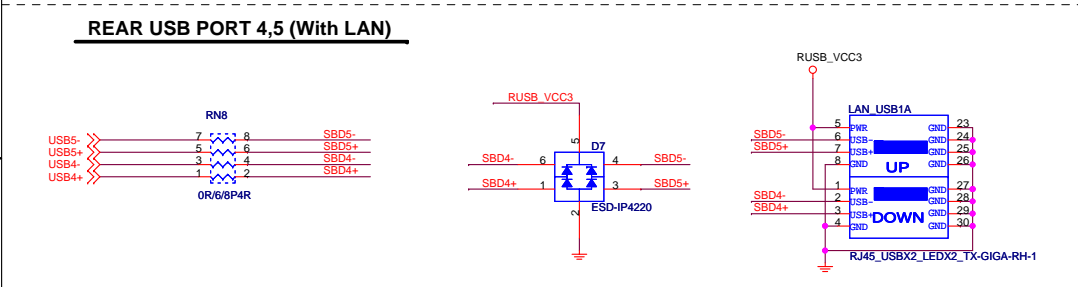
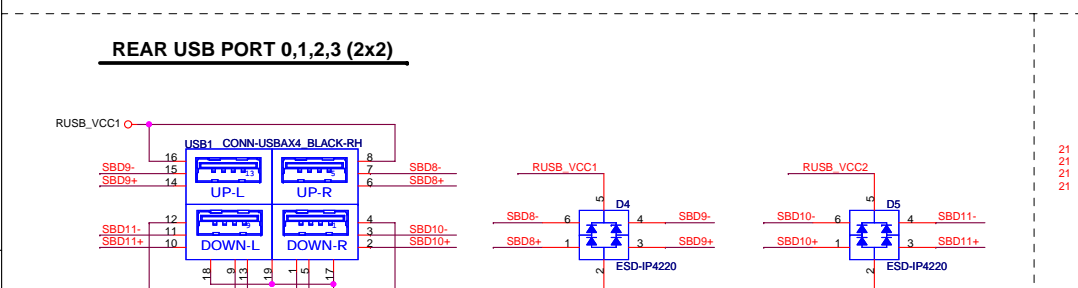
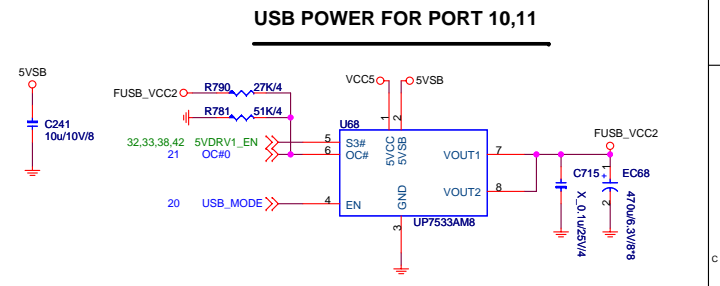
ZGPIO5 R656 X 4.7K/4
ZGPIO6 R657 X 4.7K/4
ZGPIO7 R658 X 4.7K/4
ZGPIO6 R666 X 4.7K/4
ZGPIO7 R667 X 4.7K/4



MICRO-STAR INT'L CO.,LTD			
MS-7522			
Size	Document Description	Rev	
Custom	SIH5723 - RAID SATA x2	2.0	
Date: Tuesday, October 21, 2008		Sheet	33 of 49

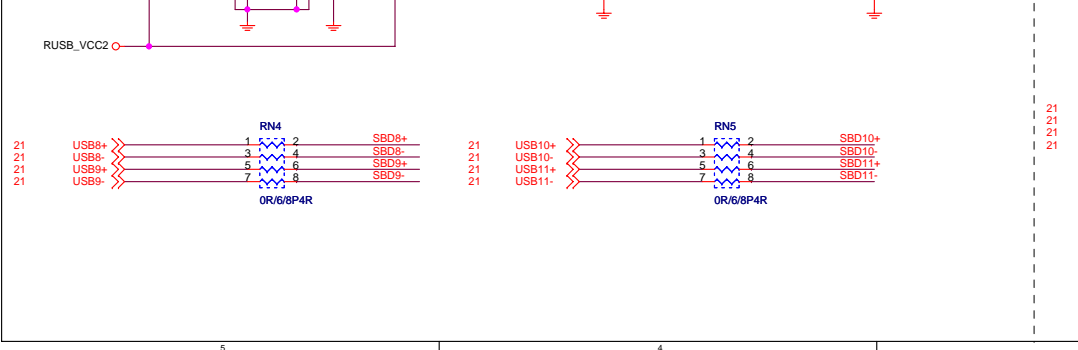
[illegible]

USB POWER FOR PORT 6,7

[illegible]

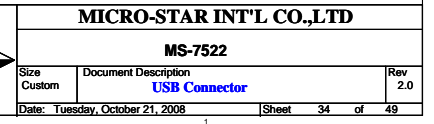
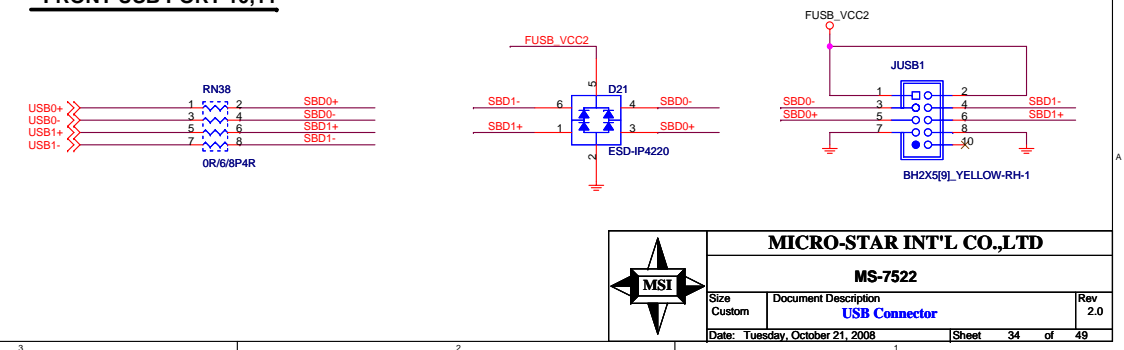
REAR USB PORT 6,7 (With LAN)

The diagram illustrates the wiring for the rear USB ports 6 and 7, which are connected to the LAN ports. The RJ45 connectors, labeled RN6 and RN7, are shown with their pin connections. RN6 pins 1, 2, 3, and 4 are connected to SBD6+, SBD6-, SBD7+, and SBD7- respectively. RN7 pins 5, 6, 7, and 8 are connected to SBD6+, SBD6-, SBD7+, and SBD7- respectively. The diagram also shows the connection to the ESD-IP4220 component, which is connected to RUSB_VCC4 and ground.

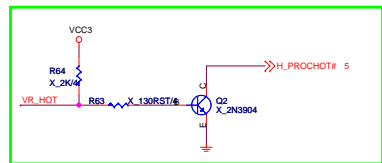
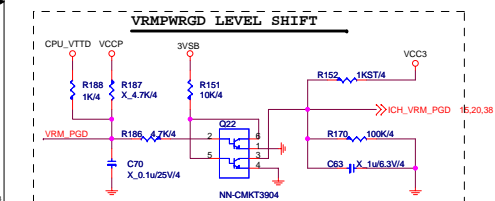
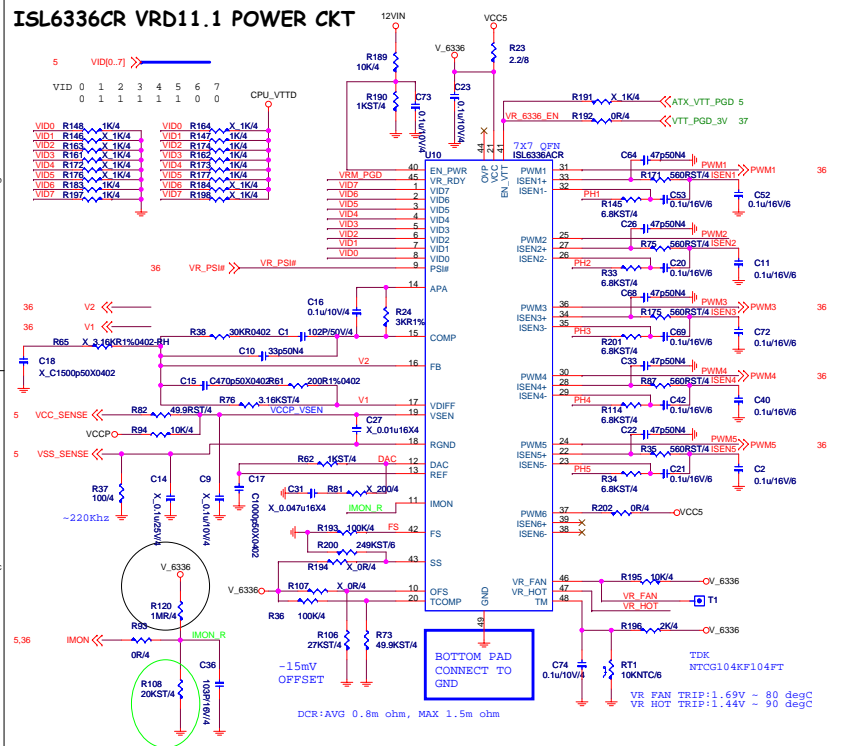


FRONT USB PORT 8,9

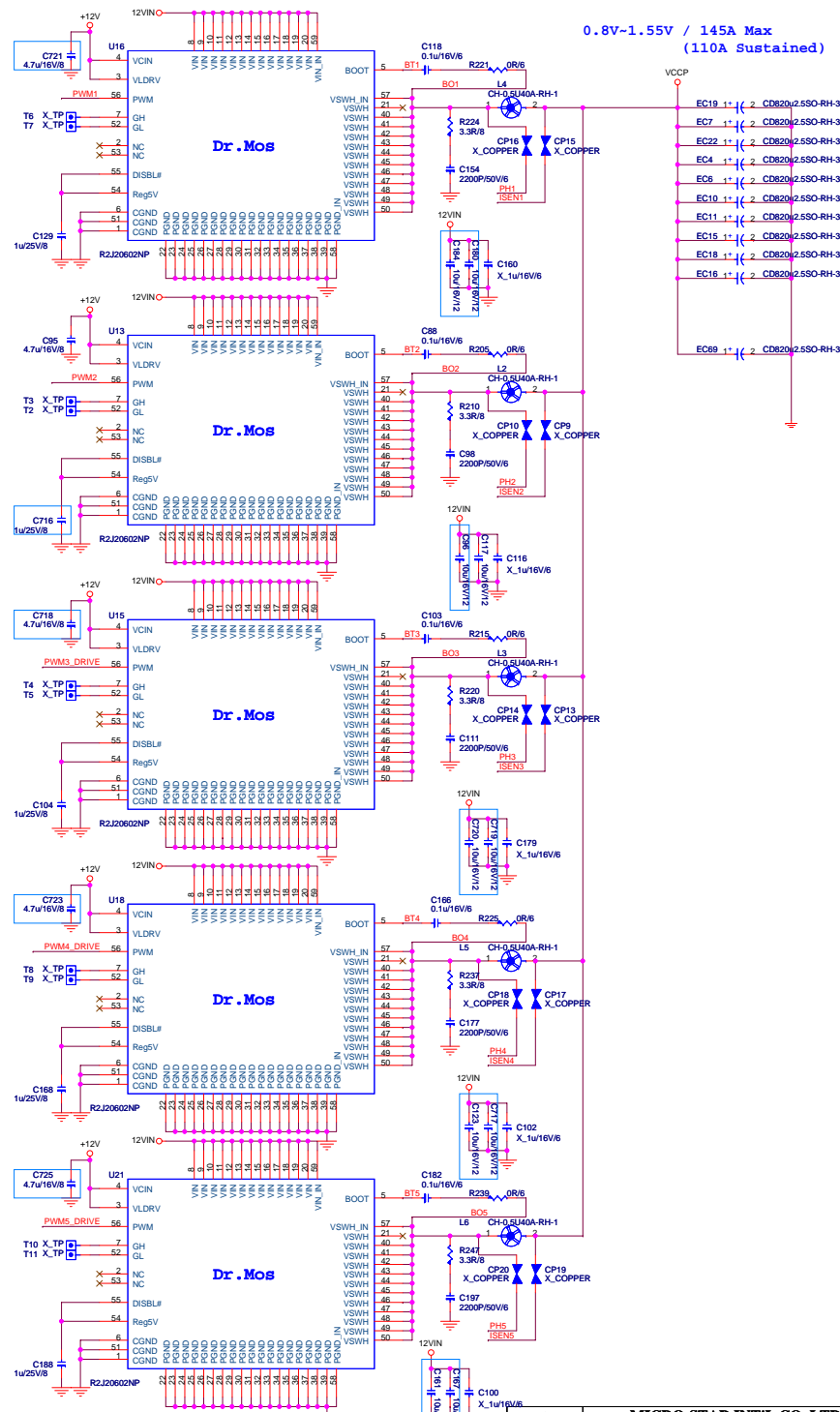
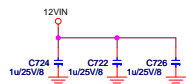
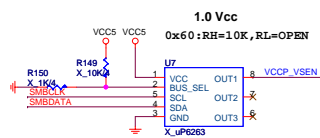
FRONT USB PORT 10 11



ISL6336CR VRD11.1 POWER CKT



UPI VOLTAGE CONSOLE



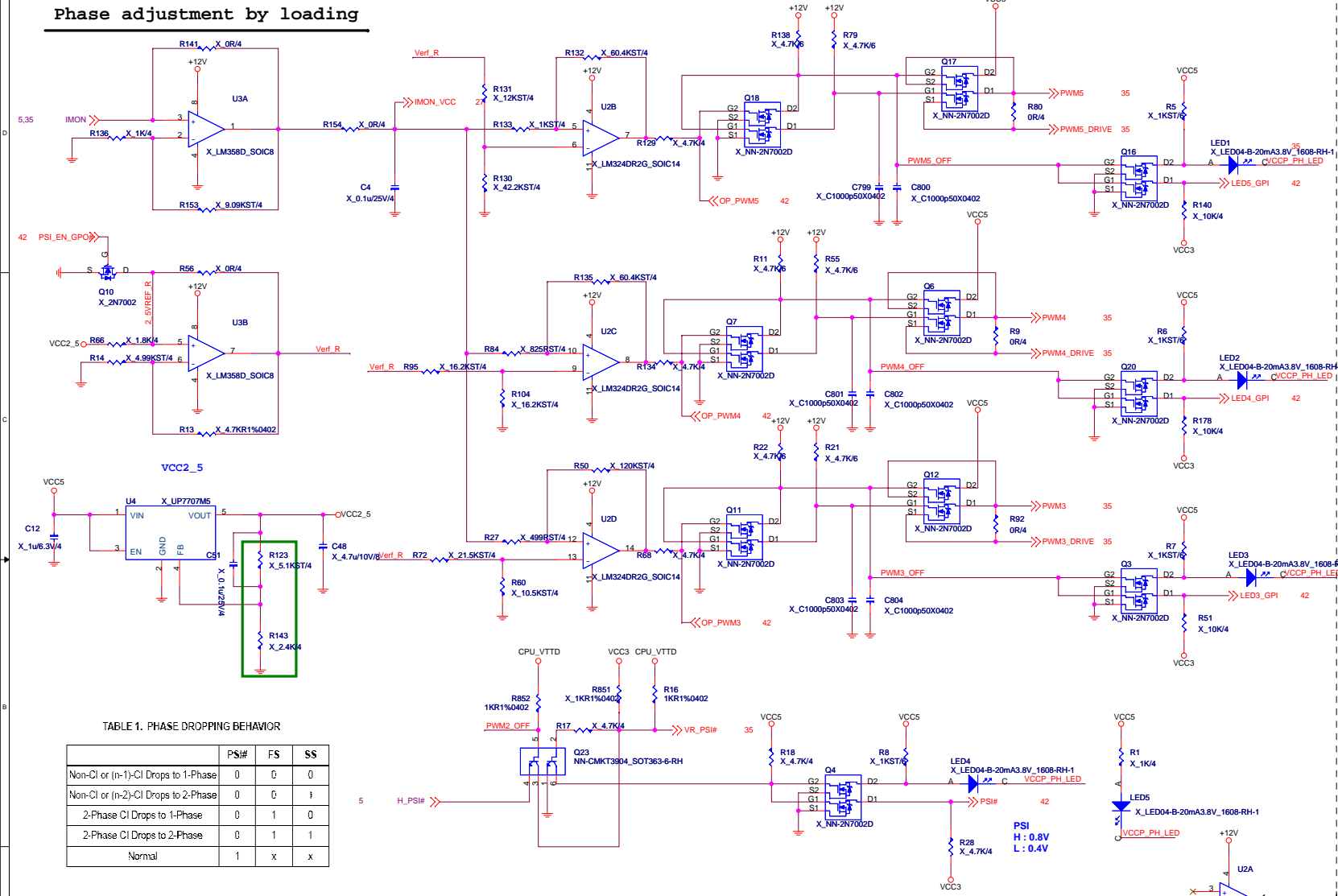
MICRO-STAR INT'L CO.,LTD

MS-7522

Size Custom	Document Description VRD11.1 - ISL6336 6-Phase
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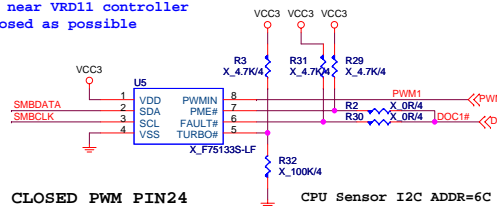
Date: Tuesday, October 21, 2008 Sheet 35 of 49

Phase adjustment by loading



EASY DOT FUNCTION

Place near VRD11 controller as closed as possible



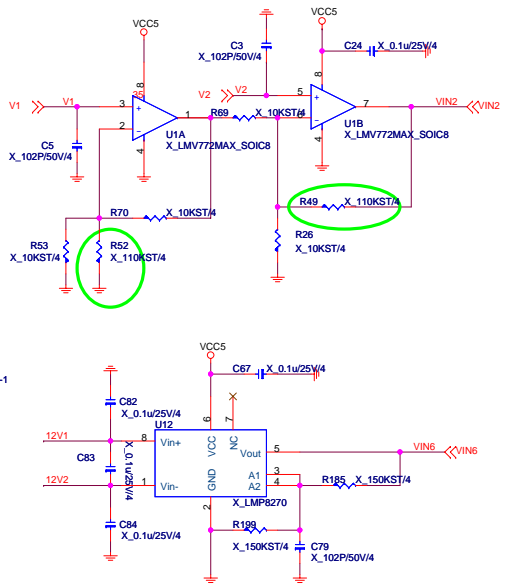
Vimon= (Riout / N) x (Rx/Risen) x Iload
 Riout = Rimon
 Rx = DCR
 Risen = ISEN+

DOC#0	DOC#1	Over-clk
1	1	15%
0	1	10%
1	0	5%
0	0	Normal

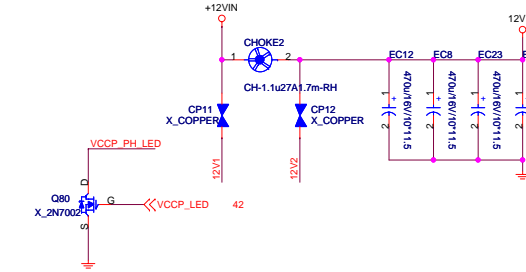
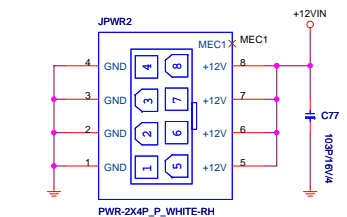
9,15,20,23,25,26,31,32,35,37,38,39,40,42,43
 9,15,20,23,25,26,31,32,35,37,38,39,40,42,43

SMBDATA SMBCLK

Power Wattage Monitor



CPU +12VIN POWER CONN.

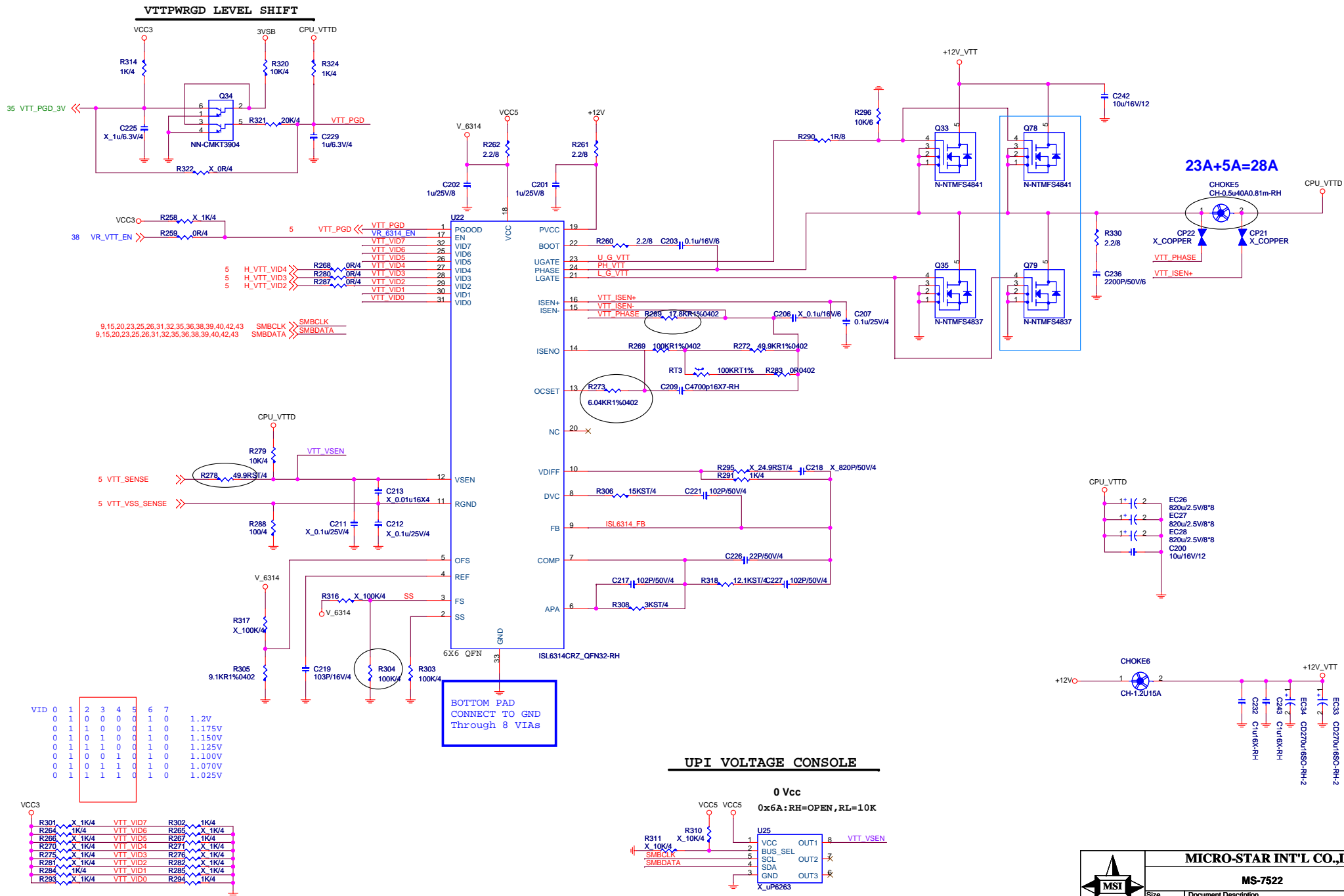


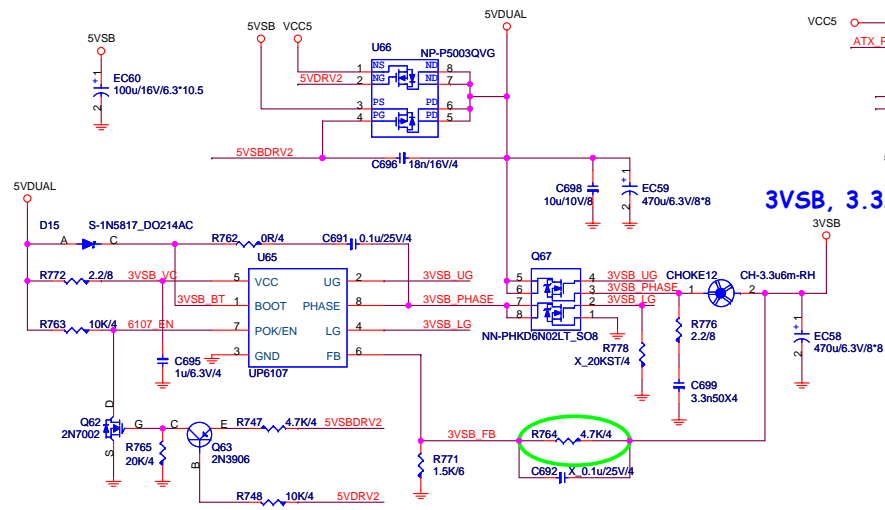
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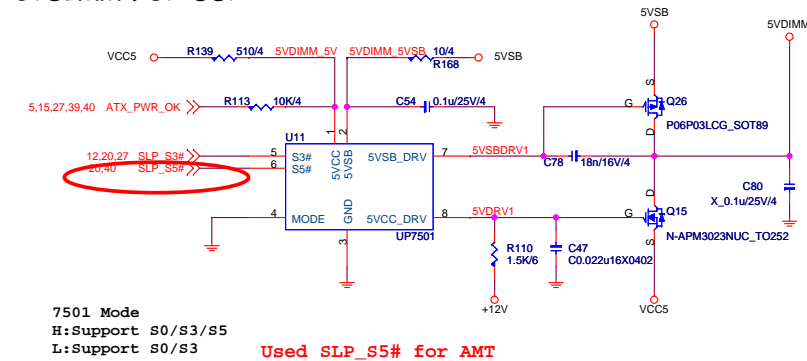
Size Custom Document Description Phase Dropping & DOT Rev 2.0
 Date: Tuesday, October 21, 2008 Sheet 36 of 49

ISL6314CR POWER CKT FOR VTT 1.1V

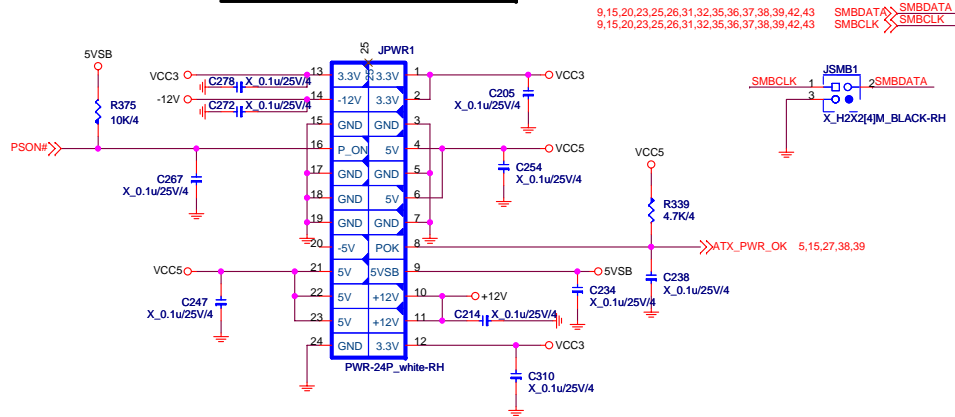




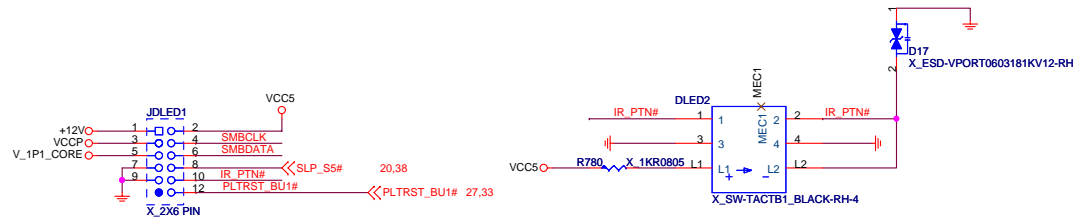
5VDIMM FOR DDR



ATX POWER CONNECTOR



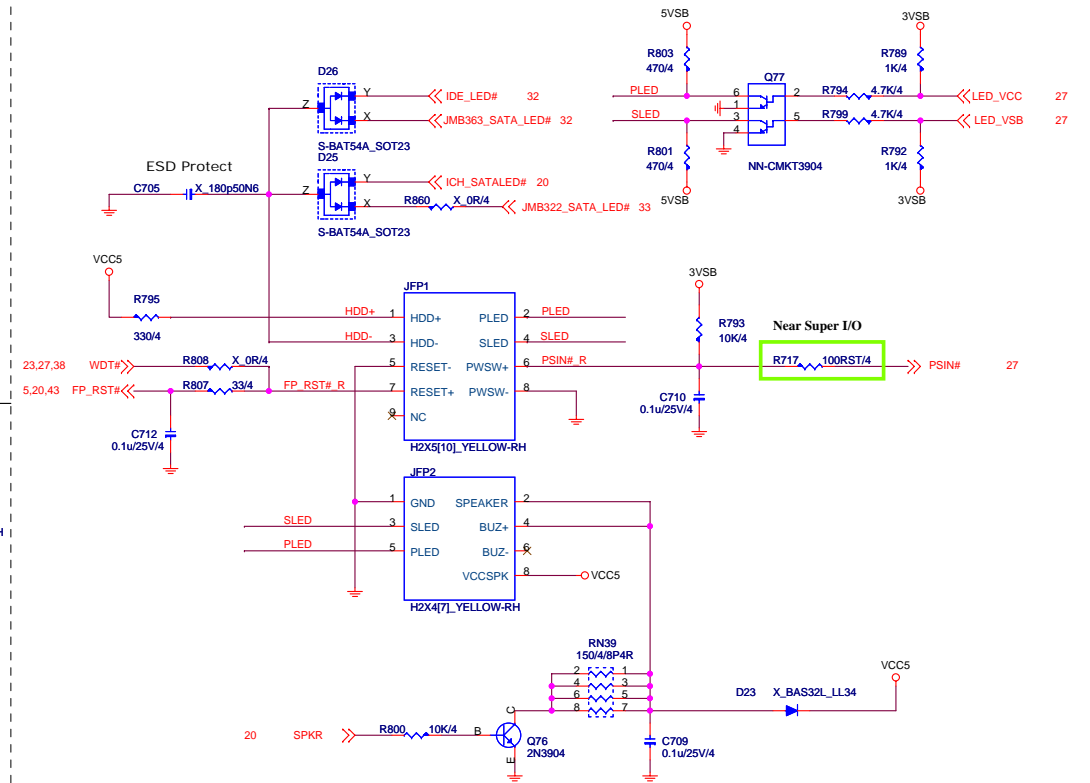
SPI Port SIN2, SOUT2 link to Super IO COM2



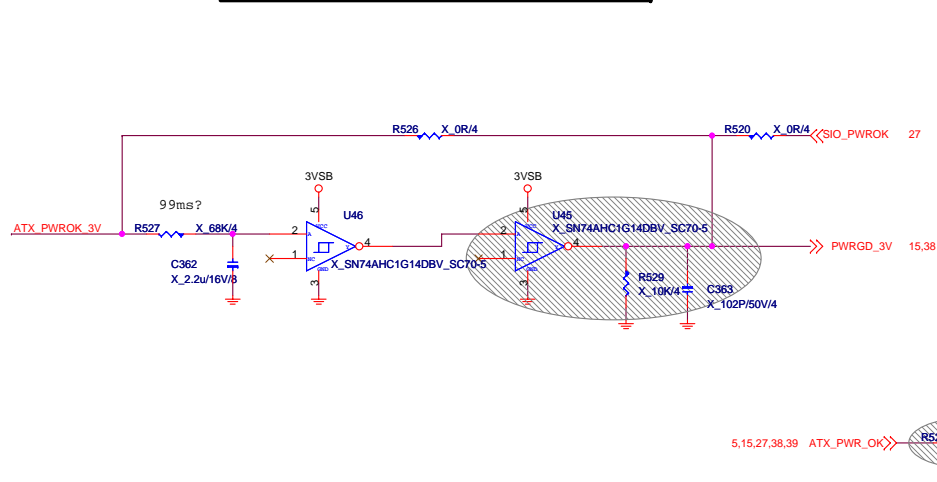
FRONT PANNEL

For MSI / Intel Front Panel

LED (By Fintek 71882)



CHIPSET POWER GOOD CIRCUIT

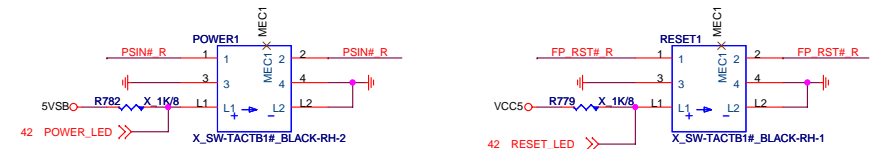


POWER ON BUTTON

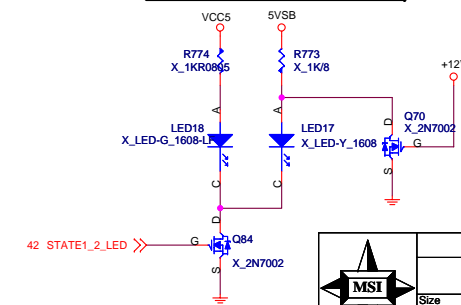
LED shine:S0 ~ S5

RESET BUTTON

LED shine:S0



POWER LED(S0/S3)



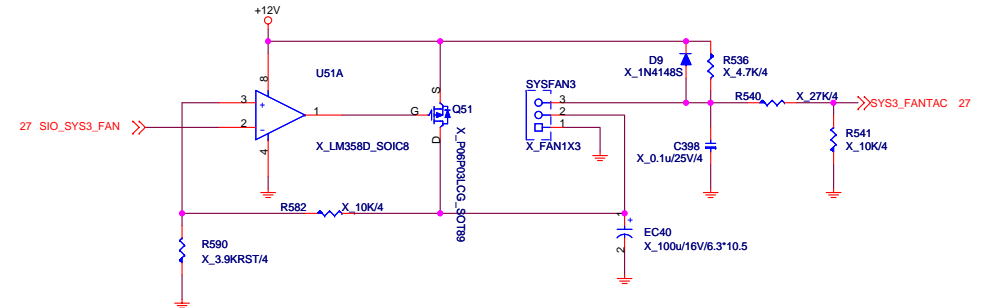
MICRO-STAR INT'L CO.,LTD

MS-7522

Size Custom	Document Description ATX Connector / Front Panel	Rev 2.0
Date: Thursday, October 23, 2008		Sheet 40 of 49

The diagrams show the pin connections for three SATA ports (SATA1, SATA2, and SATA5) to the SATA14PM_PURPLE-RH and SATA14PM_PINK-RH connectors. Each port has a 15-pin header and a 16-pin connector. The connections are as follows:

- SATA1:**
 - Pin 1: GND to GND
 - Pin 2: HT+1 to HT+2
 - Pin 3: HT-1 to HT-2
 - Pin 4: GND to GND
 - Pin 5: GND to GND
 - Pin 6: HR+1 to HR+2
 - Pin 7: HR-1 to HR-2
 - Pin 8: GND to GND
 - Pin 9: MEC1 to MEC2
 - Pin 10: ST TX1 to C396
 - Pin 11: ST TX#1 to C400
 - Pin 12: ST RX#1 to C410
 - Pin 13: ST RX1 to C415
 - Pin 14: 103P16V/4 to 103P16V/4
 - Pin 15: 103P16V/4 to 103P16V/4
 - Pin 16: 103P16V/4 to 103P16V/4
- SATA2:**
 - Pin 1: GND to GND
 - Pin 2: HT+1 to HT+2
 - Pin 3: HT-1 to HT-2
 - Pin 4: GND to GND
 - Pin 5: GND to GND
 - Pin 6: HR+1 to HR+2
 - Pin 7: HR-1 to HR-2
 - Pin 8: GND to GND
 - Pin 9: MEC1 to MEC2
 - Pin 10: ST TX3 to C474
 - Pin 11: ST TX#3 to C479
 - Pin 12: ST RX#3 to C484
 - Pin 13: ST RX3 to C489
 - Pin 14: 103P16V/4 to 103P16V/4
 - Pin 15: 103P16V/4 to 103P16V/4
 - Pin 16: 103P16V/4 to 103P16V/4
- SATA5:**
 - Pin 1: GND to GND
 - Pin 2: HT+1 to HT+2
 - Pin 3: HT-1 to HT-2
 - Pin 4: GND to GND
 - Pin 5: GND to GND
 - Pin 6: HR+1 to HR+2
 - Pin 7: HR-1 to HR-2
 - Pin 8: GND to GND
 - Pin 9: MEC1 to MEC2
 - Pin 10: ST TX5 to C532
 - Pin 11: ST TX#5 to C534
 - Pin 12: ST RX#5 to C539
 - Pin 13: ST RX5 to C541
 - Pin 14: 103P16V/4 to 103P16V/4
 - Pin 15: 103P16V/4 to 103P16V/4
 - Pin 16: 103P16V/4 to 103P16V/4



FAN-COUNTDOWN CIRCUIT

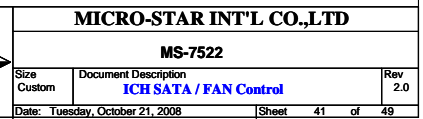
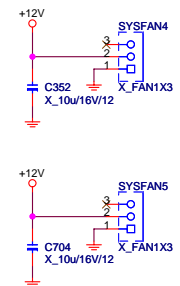
The schematic diagram illustrates the FAN-COUNTDOWN CIRCUIT, which consists of two identical sections for SYS1_FANTAC and SYS2_FANTAC.

Section 1 (SYS1_FANTAC):

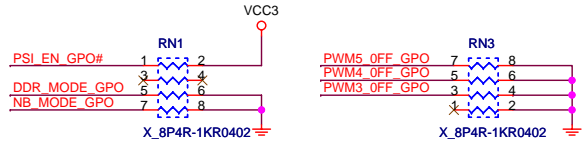
- The input signal **27_SIO_SYS1_FAN** is connected to the non-inverting input (pin 10) of the op-amp **U44C** (LM324DR2G_SOIC14).
- The op-amp's output (pin 8) is connected to the gate (pin G) of the MOSFET **Q50** (P06P03LCG_SOT89).
- The MOSFET's source (pin S) is connected to ground.
- The MOSFET's drain (pin D) is connected to a +12V supply through a resistor **R528** (4.7K/4).
- A diode **D8** (1N4148S) is connected in parallel with the MOSFET's drain.
- A resistor **R535** (27K/4) is connected between the MOSFET's drain and the output signal **SYS1_FANTAC**.
- A resistor **R543** (10K/4) is connected between the MOSFET's gate and the output signal.
- A resistor **R544** (3.9KRST/4) is connected between the MOSFET's gate and ground.
- A capacitor **C397** (X_0.1u/25V/4) is connected between the MOSFET's gate and ground.
- A capacitor **EC39** (100u/16V/6.3*10.5) is connected between the MOSFET's drain and ground.
- The output signal is **SYS1_FANTAC**.

Section 2 (SYS2_FANTAC):

- The input signal **27_SIO_SYS2_FAN** is connected to the non-inverting input (pin 12) of the op-amp **U44D** (LM324DR2G_SOIC14).
- The op-amp's output (pin 14) is connected to the gate (pin G) of the MOSFET **Q61** (P06P03LCG_SOT89).
- The MOSFET's source (pin S) is connected to ground.
- The MOSFET's drain (pin D) is connected to a +12V supply through a resistor **R696** (4.7K/4).
- A diode **D12** (1N4148S) is connected in parallel with the MOSFET's drain.
- A resistor **R698** (27K/4) is connected between the MOSFET's drain and the output signal **SYS2_FANTAC**.
- A resistor **R545** (10K/4) is connected between the MOSFET's gate and the output signal.
- A resistor **R546** (3.9KRST/4) is connected between the MOSFET's gate and ground.
- A capacitor **C590** (X_0.1u/25V/4) is connected between the MOSFET's gate and ground.
- A capacitor **EC51** (100u/16V/6.3*10.5) is connected between the MOSFET's drain and ground.
- The output signal is **SYS2_FANTAC**.

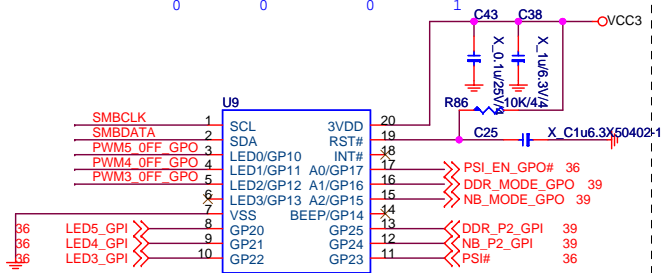



GPIO Controller

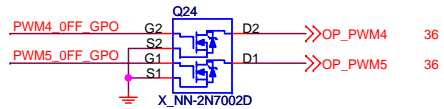
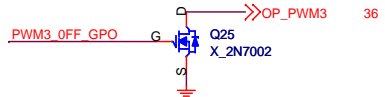


Programming
Default GPI ==>GPO(O/D)==>GPO(O)==>GPO(O)

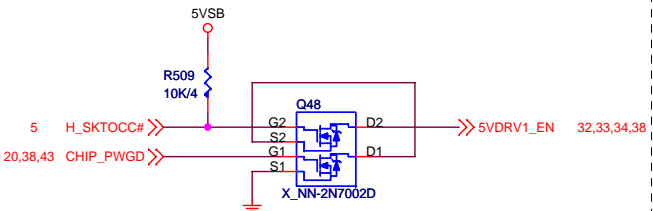
0	0	0	1
---	---	---	---



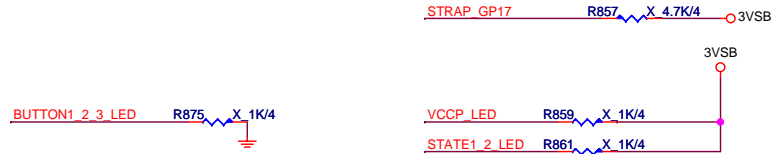
Only PSI_EN_GPO Default High
Others Default Low



防測試線路



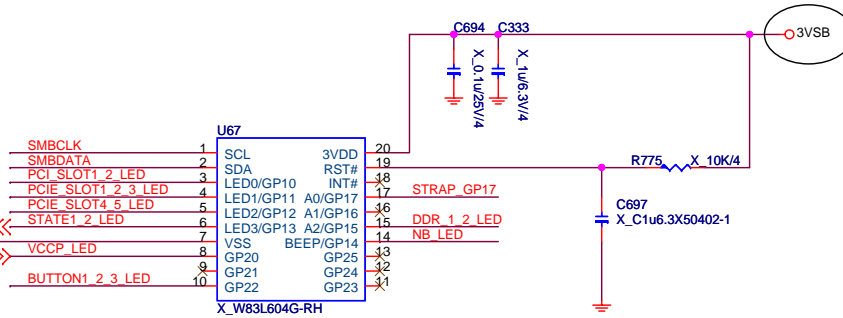
GPIO Controller - B LED / VTT / PHASE6



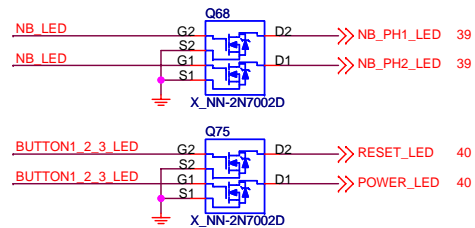
```

Programming
Default GPI ==>GPO(O/D)==>GPO(O)==>GPO(O)
           0           0           0           1

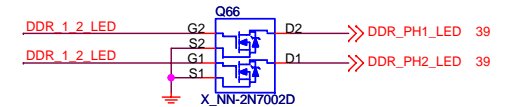
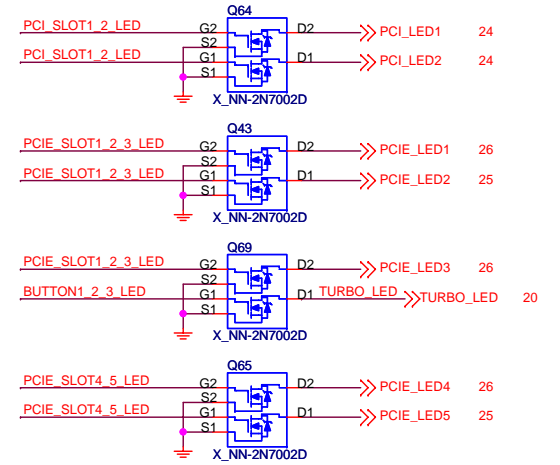
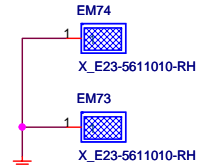
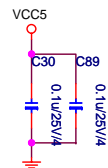
```



Only VTT_PSI_GPO# Default High
Others Default Low



EMI CAP

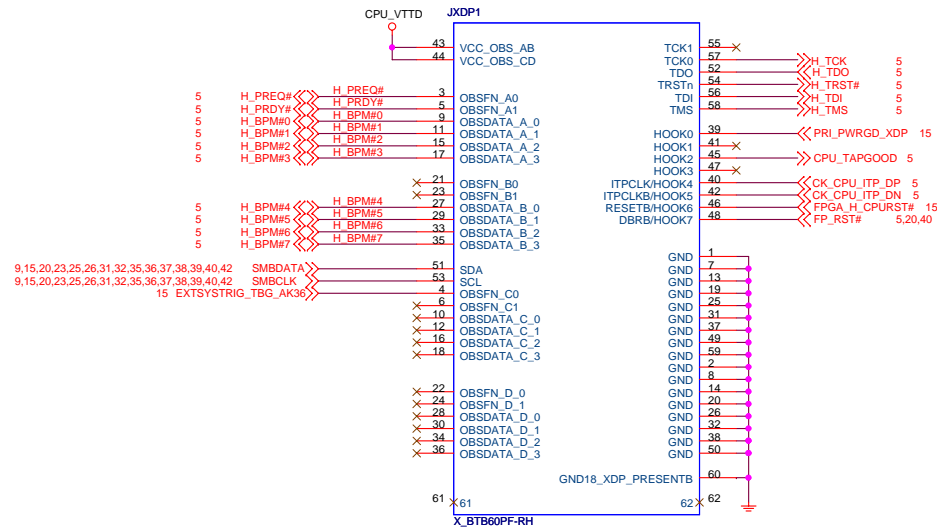


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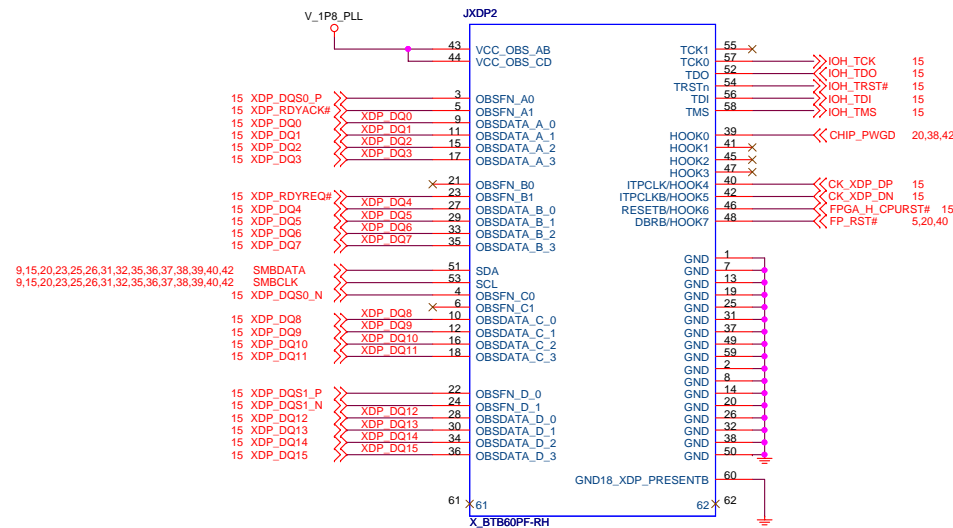
MS-7522

Size Custom	Document Description GPIO Controller/EMI	Rev 2.0
Date: Tuesday, October 21, 2008		Sheet 42 of 49

Reserve debug port 5020

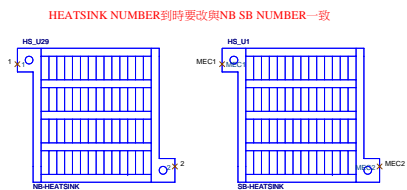


Reserve debug port 5020





PD0-0752220-G37, 精成
PD0-0752220-E48, 競華



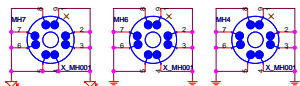
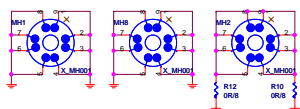
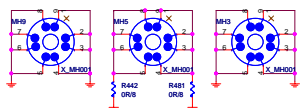
Optical Fiducial Marks-120



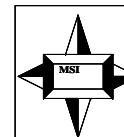
Optical Fiducial Marks-100



Mounting Holes



Simulation



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MS-7522

Size	Document Description	Rev
Custom	Manual Parts	2.0
Date	Friday, October 24, 2008	Sheet 44 of 49